15W,28V Plastic RF LDMOS Transistor

ITEH25015P3

Description

The ITEH25015P3 is a 15-watt, highly rugged, LDMOS transistor, designed for any general applications at frequencies up to 2.5GHz, in 6*5mm DFN plastic package, supporting surface mounted on PCB through high density grounding vias.

•Typical **UHF** Class AB RF Performance (On Innogration fixture with device soldered).

VDS=**28V**, IDQ=100mA Pulsed CW: 100 us width, 20% duty cycle.

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
700	42.4	17.4	63.1	17.96	43.64	23.1	69.1
800	42.44	17.6	63.4	18.75	43.72	23.5	69.8
900	42.31	17.0	63.9	19.09	43.54	22.6	69.4
960	42.01	15.9	64.7	18.33	43.29	21.3	69.2

•Typical **L band** Class AB RF Performance (On Innogration fixture with device soldered).

VDS=**28V**, IDQ=100mA Pulsed CW: 100 us width, 20% duty cycle.

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
1200	42.73	18.7	54.2	17.96	43.71	23.5	59.2
1300	42.61	18.3	57.0	18.25	43.48	22.3	60.9
1400	42.24	16.8	61.4	18.07	43.12	20.5	64.8
1500	41.86	15.3	63.8	17.39	42.67	18.5	65.5
1600	41.34	13.6	61.1	16.05	42.21	16.6	61.1

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- Broadcast and Industrial, Scientific and Medical applications in the frequency range from HF to 2.5GHz
- All 4G/5G cellular application below 2.5GHz

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+65	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+28	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.2	°C/W

T_C= 85°C, Pout=15W 2GHz			

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

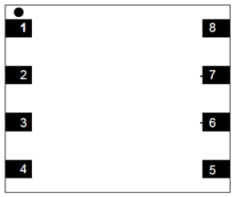
Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage V_{GS}=0, I_{DS}=100uA	$V_{(BR)DSS}$		65		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate--Source Leakage Current (V_{GS} = 11 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 28V, I_D = 600 μA)	$V_{GS(th)}$	——	2	——	V
Gate Quiescent Voltage (V_{DD} = 28V, I_D = 100mA, Measured in Functional Test)	$V_{GS(Q)}$	——	2.4	——	V

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 28Vdc, I_{DQ} = 100 mA, f = 2100 MHz

VSWR 10:1 at 10W pulse CW Output Power	No Device Degradation

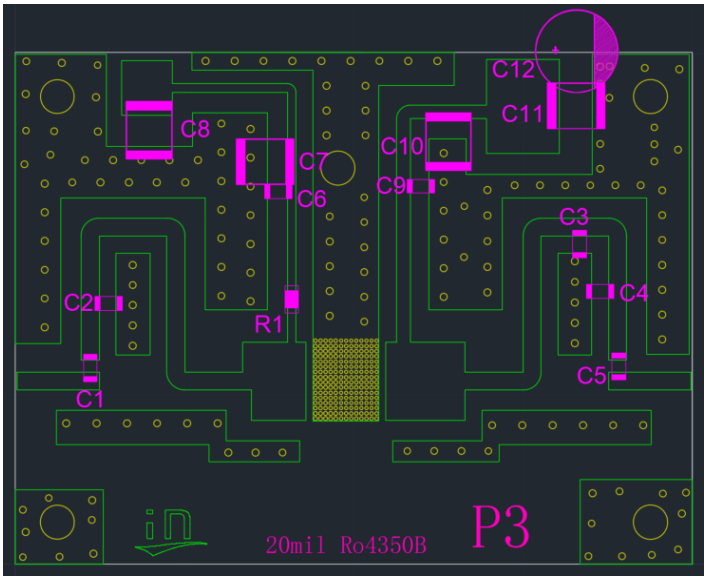
Pin Configuration and Description(Top view)



Pin No.	Symbol	Description
1,2,3,4	RF IN/VGS	Gate Bias/RF Input
5,6, 7,8	RF OUT /VDS	RF Output, Drain Bias
Backside metal	GND	DC/RF Ground. Must be soldered to EVB ground plane over array of vias for thermal and RF performance. Solder voids under Pkg Base will result in excessive junction temperatures causing permanent damage.

700-960MHz

Reference Circuit of Test Fixture Assembly Diagram 20mils RO4350B

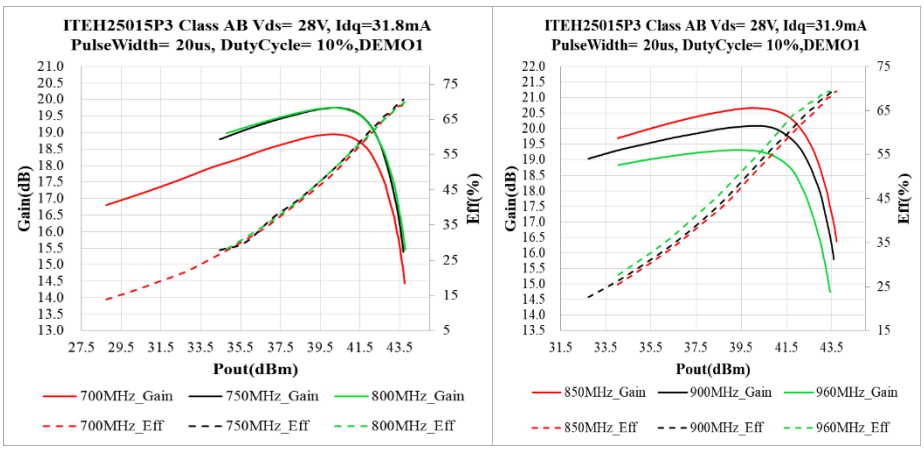


Test Circuit Component Layout

Reference	Footprint	Value	Quantity
C1	0603	4.7 pF	1
C2,C3,C4	0603	2 pF	3
C5,C6,C9	0603	100 pF	3
C7,C8,C10,C11	1210	10 uF/63V	4
C12	/	470 uF	1
R1	0603	10 ohm	1
U1	P3	ITEH25015P3	1

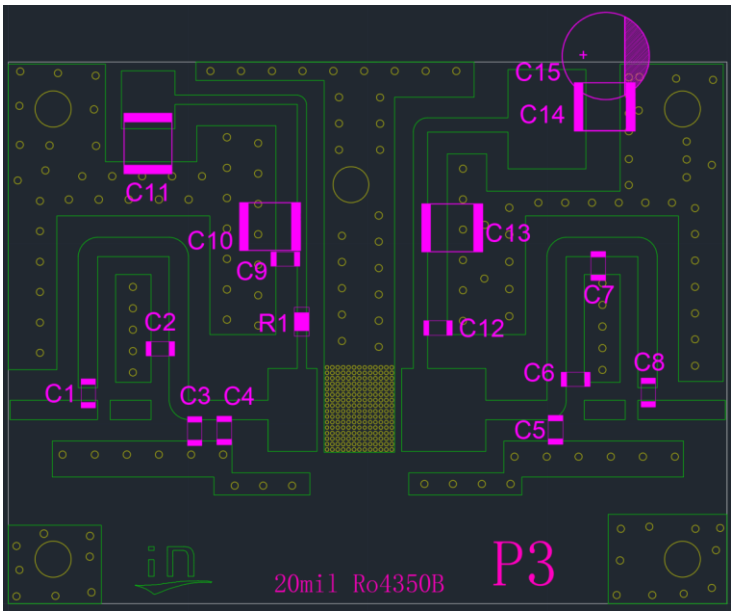
TYPICAL CHARACTERISTICS

Figure 3. Power Gain and Drain Efficiency as function of Power Output



1200-1600MHz

Reference Circuit of Test Fixture Assembly Diagram 20mils RO4350B

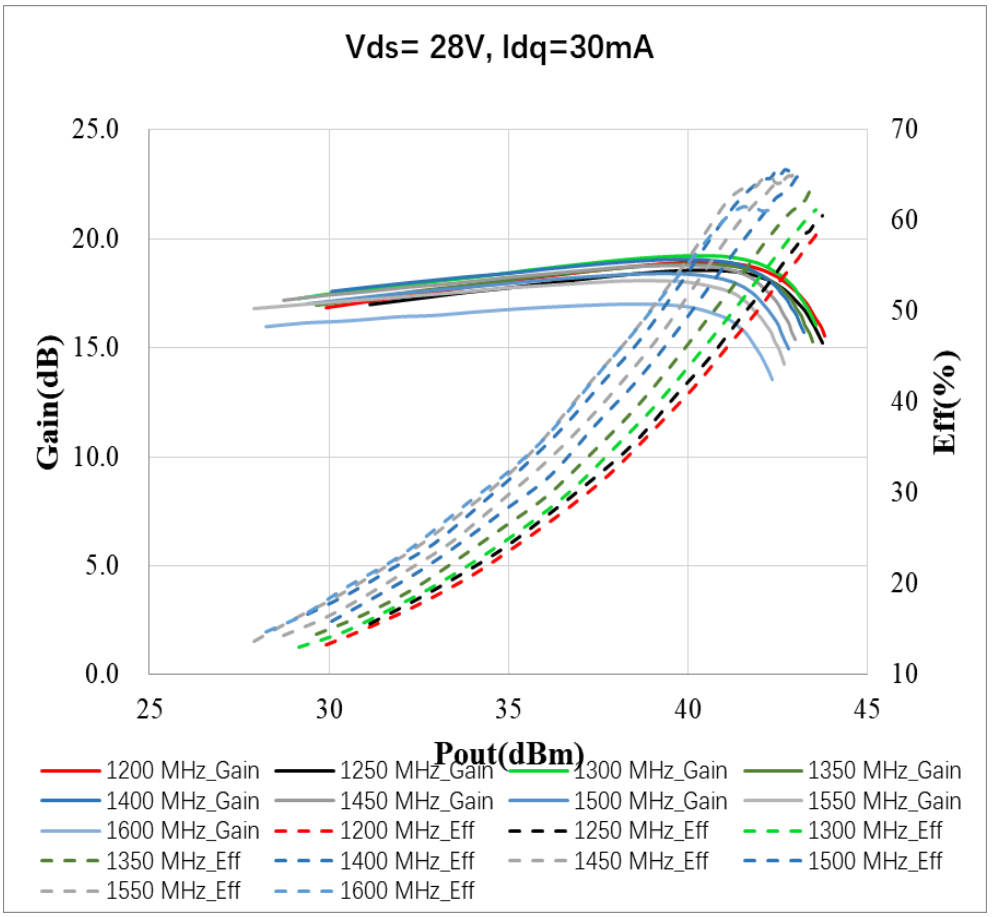


Test Circuit Component Layout

Reference	Footprint	Value	Quantity
C1	0603	4.7 pF	1
C2,C5	0603	2.4 pF	2
C3	0603	4.3 pF	1
C4	0603	1.5 pF	1
C6,C7	0603	2 pF	2
C8,C9,C12	0603	47 pF	3
C10,C11,C13,C14	1210	10 uF/63V	4
C15	/	470 uF	1
R1	0603	10 ohm	1

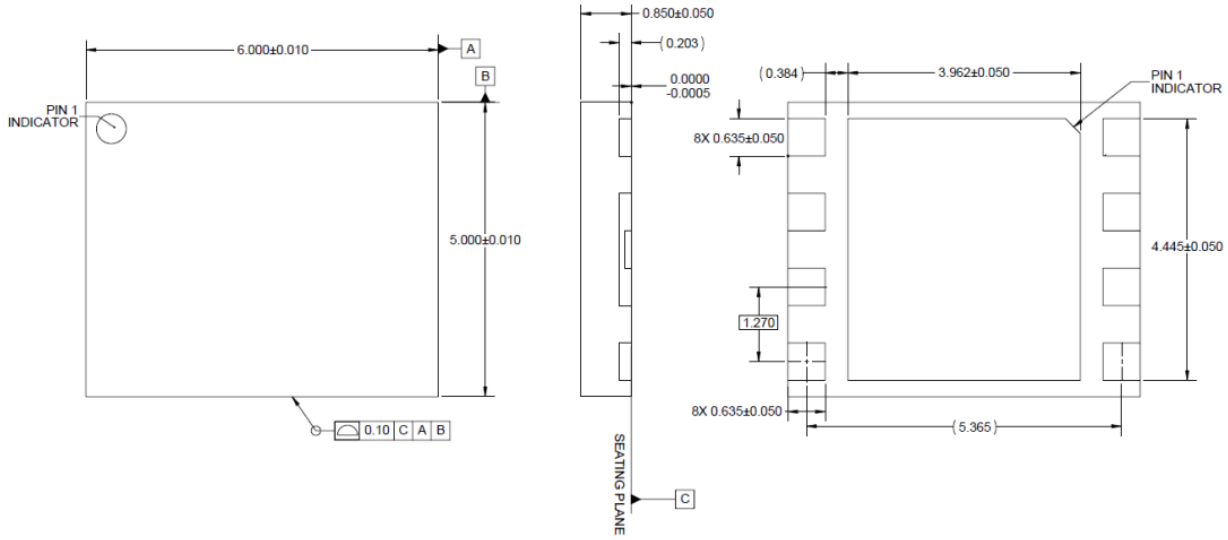
TYPICAL CHARACTERISTICS

Figure 4. Power Gain and Drain Efficiency as function of Power Output



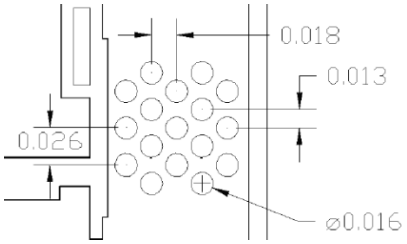
Package Outline

6*5 DFN Package



Notes:
1. All dimensions are in mm. Otherwise noted, the tolerance is ±0.1 mm.
2. Package leads are gold plated.
3. Part is mold encapsulated.

Recommended vias layout: (all in inches)



Revision history

Table 7. Document revision history

Date	Revision	Datasheet Status
2025/11/8	Rev 1.0	Preliminary Datasheet

Application data based on CWZ-25-19/20

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