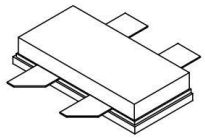
ITEV011K1BY4 LDMOS TRANSISTOR

Document Number: ITEV011K1BY4
Preliminary Datasheet V1.0

1000W, 50V High Power RF LDMOS FETs

ITEV011K1BY4



Description

The ITEV011K1BY4 is a 1000-watt capable, high performance, unmatched LDMOS FET, designed for HF/VHF. It can be used for both CW and pulse application.

It is featured for high power and high ruggedness, low cost, suitable for ISM RF Energy application.

- Typical Performance (On Innogration 108MHz fixture with device soldered):

ITEV011K1BY4 VGS=3.17V VDS=50V IDQ=450mA						
Signal	Pout(dBm)	Pout(W)	Pin(dBm)	Gain(dB)	Eff(%)	$2^{nd}/3^{rd}$ harmonic(dB)
CW	60.3	1070	41.5	18.8	84	-21/-13

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- On chip RC network enable high stability and ruggedness
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Excellent thermal stability, low HCI drift
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	135	Vdc
Gate--Source Voltage	V_{GS}	-7 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case ,Case Temperature 80°C, 1000W CW, 50 Vdc, I_{DQ} = 200 mA	$R_{\theta JC}$	0.18	°C/W
Transient thermal impedance from junction to case Tj = 150° C; tp = 100 us; Duty cycle = 10 %	Zth	0.045	°C/W

Table 3. ESD Protection Characteristics

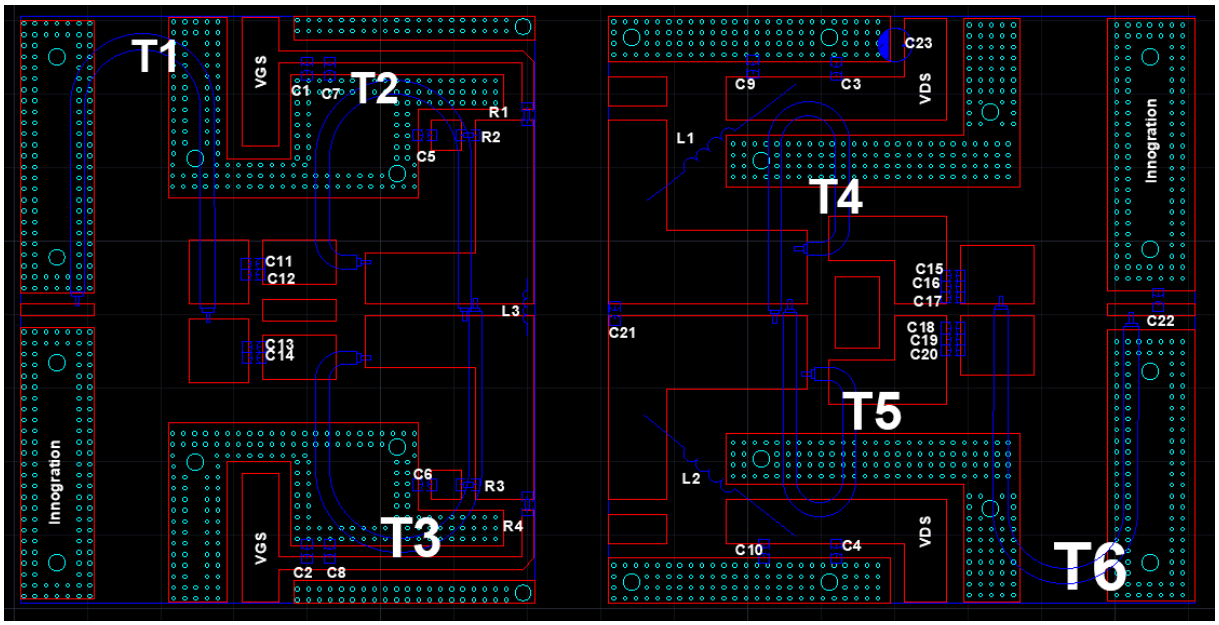
Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics (Per Side)					
Drain-Source Voltage V_{GS}=0, I_{DS}=18.0mA	$V_{(BR)DSS}$		135		V

Zero Gate Voltage Drain Leakage Current (V_{DS} = 50V, V_{GS} = 0 V)	I_{DSS}			1	μA
Gate—Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}			1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600 μA)	$V_{GS(th)}$		2.6		V
Gate Quiescent Voltage (V_{DD} = 50 V, I_D =450 mA, Measured in Functional Test)	$V_{GS(Q)}$		3.17		V
Common Source Input Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz) Each section side of device measured	C_{ISS}		375		pF
Common Source Output Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz) Each section side of device measured	C_{OSS}		108		pF
Common Source Feedback Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz) Each section side of device measured	C_{RSS}		2.4		pF

Reference Circuit of Test Fixture (108MHz)



Component	Description	Suggestion
C1~C6	10uF/200V-1210	Ceramic multilayer capacitor
C7~10	10nF/200V-1210	Ceramic multilayer capacitor
C11~C14	150pF	
C15~C20	560pF	
C21	24pF	
C22	12pF	mica capacitor
C23	4700uF/63V	electrolytic capacitor

T1	50 ohm-150mm	RFSFBU-086-50
T2,T3	25 ohm-150mm	RFSFBU-086-25
T4,T5	12.5 ohm-130mm	SFF-12.5-3
T6	50 ohm-150mm	SFF-50-3
R1,R4	300Ω-1206	Chip Resistor
R2,R3	51Ω-2512	Chip Resistor
L1,L2	1.5mm wire ， 5mm inner diameter， 5 Turns	DIY
L3	1.5mm wire ， 5mm inner diameter， 3 Turns	DIY

Typical performance

Figure 1：Power Gain，Efficiency as function of Pout

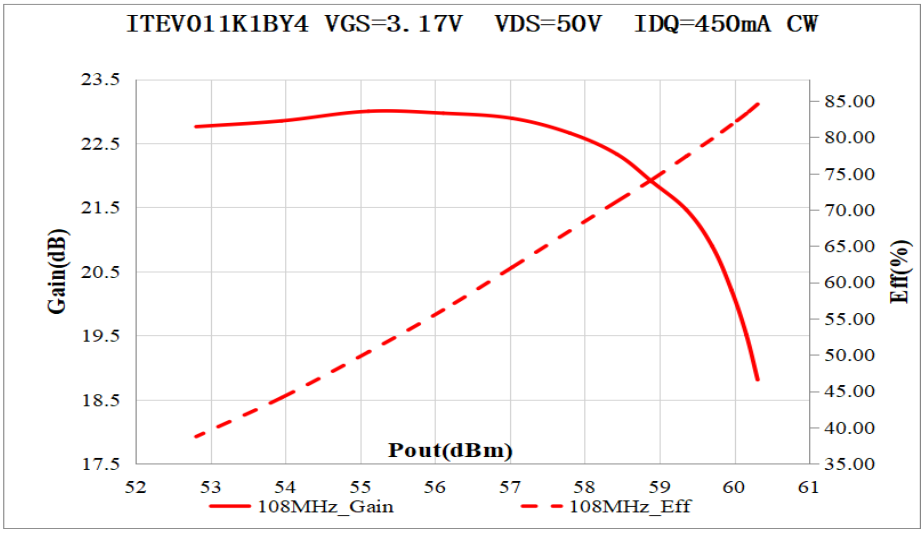
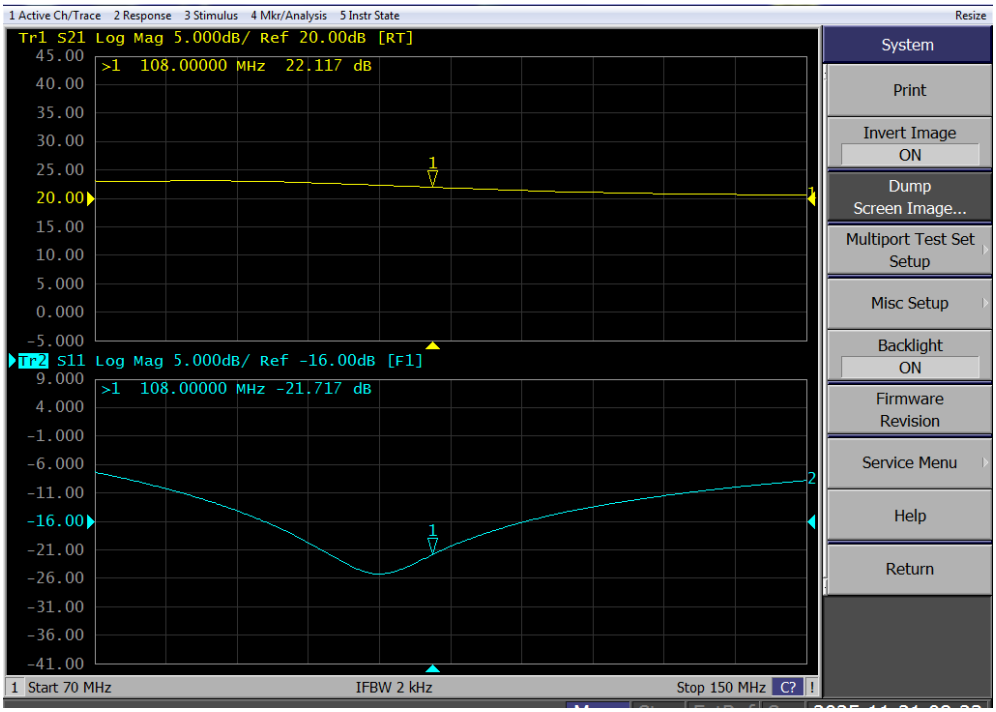
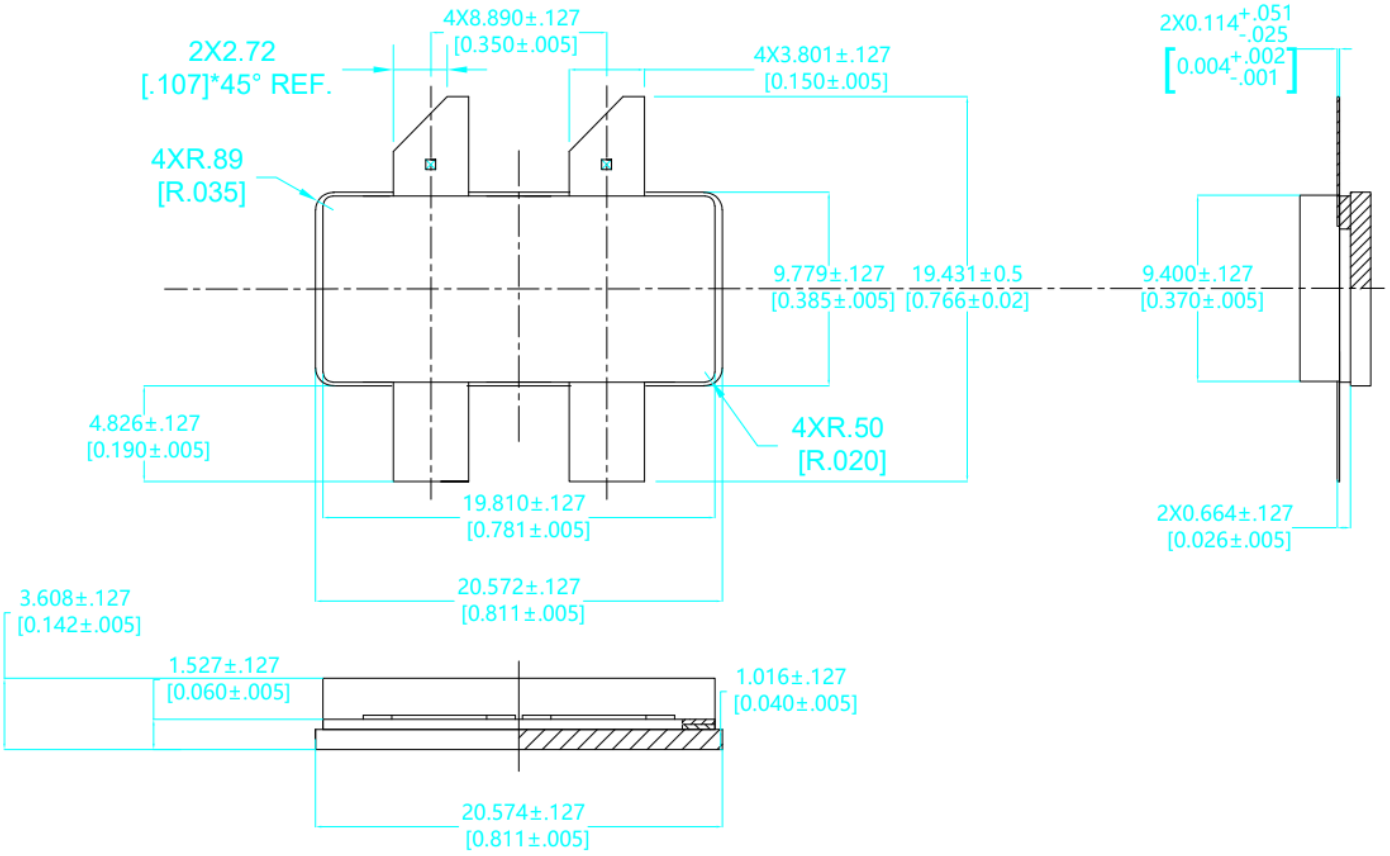


Figure 2：Network analyzer output S11/S21, Pin=0dBm



Earless Flanged Ceramic Package; 4 leads



OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-BY4					07/27/2023

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2025/11/24	Rev 1.0	Preliminary Datasheet

Application data based on TC-25-40

Disclaimers