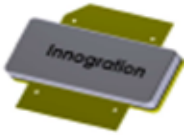
MC011K5VXS*2 LDMOS TRANSISTORs

Document Number: MC011K5VXS
Preliminary Datasheet V1.0

3000W, 50V High Power RF LDMOS Paired FETs

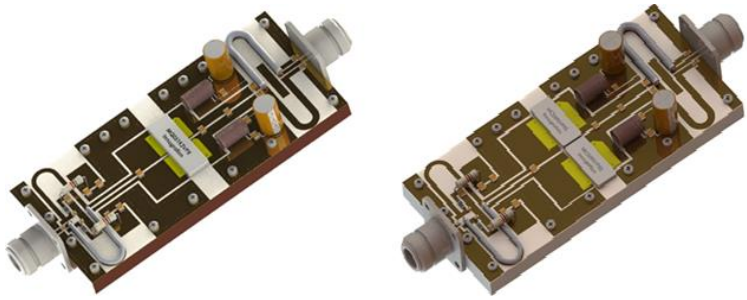
MC011K5VXS



Description

The MC011K5VXS itself is a 1500watt capable, high performance, unmatched single ended and earless LDMOS FET.**It is recommended to use paired MC011K5VXS to enable industry leading RF power up to 3000W at 50V, for ISM applications within frequencies HF to 150MHz.** Compared to equivalent dual-path packaged device, it offers better thermal management and easier maintenance, while maintaining the same size.

Demonstration of paired MC011K5VXS(right) Vs single dual-path device(left) mounted on the same design as below



- Typical performance(on 108MHz narrow band application board with **2*MC011K5VXS** devices soldered)

V_{DS}=50V,I_{DQ}=1000mA, Pulsed CW, 10% duty cycle, 100us pulse width

Vds	Pin(dBm)	Pout(W)	IDS(A)	Gain(dB)	Eff(%)
50	48.4	3150	9.35	16.6	76

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 136-174MHz (Commercial ground communication)
- Laser Exciter
- Synchrotron
- MRI
- Plasma generator
- Weather Radar

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+140	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Transient thermal impedance from junction to case Tj = 85° C; tp = 100 us; Duty cycle = 10 %	Zth	0.013	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (T_A = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics (per half section)					
Drain-Source Voltage V_{GS}=0, I_{DS}=1.0mA	$V_{(BR)DSS}$		140		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 75V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50 V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate--Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600 μA)	$V_{GS(th)}$	——	2.0	——	V
Gate Quiescent Voltage (V_{DD} = 50 V, I_D = 500 mA, Measured in Functional Test)	$V_{GS(Q)}$	——	3.1	——	V

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 50 Vdc, I_{DQ} = 1000 mA, f = 100MHz, pulse width:100us, duty cycle:10%, 2 piece of MC011K5VXS combined

65：1, at 3000W Pulsed CW Output Power	No Device Degradation

Reference Circuit of Test Fixture (108MHz Power Amplifier)

Note: This demo board is used for short time demonstration only, for long time CW operation, heat management for some components might needed

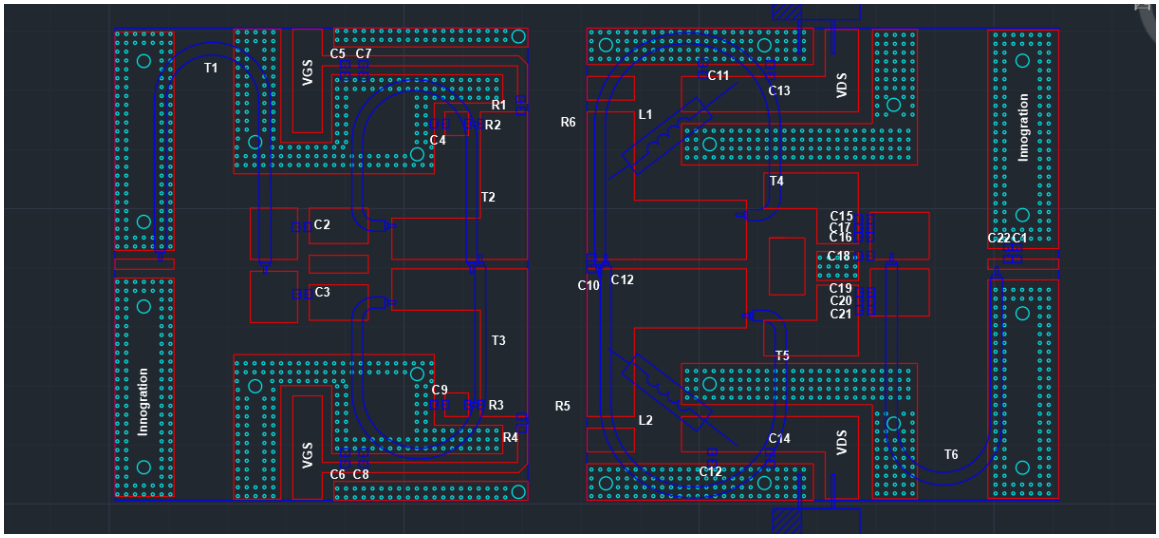
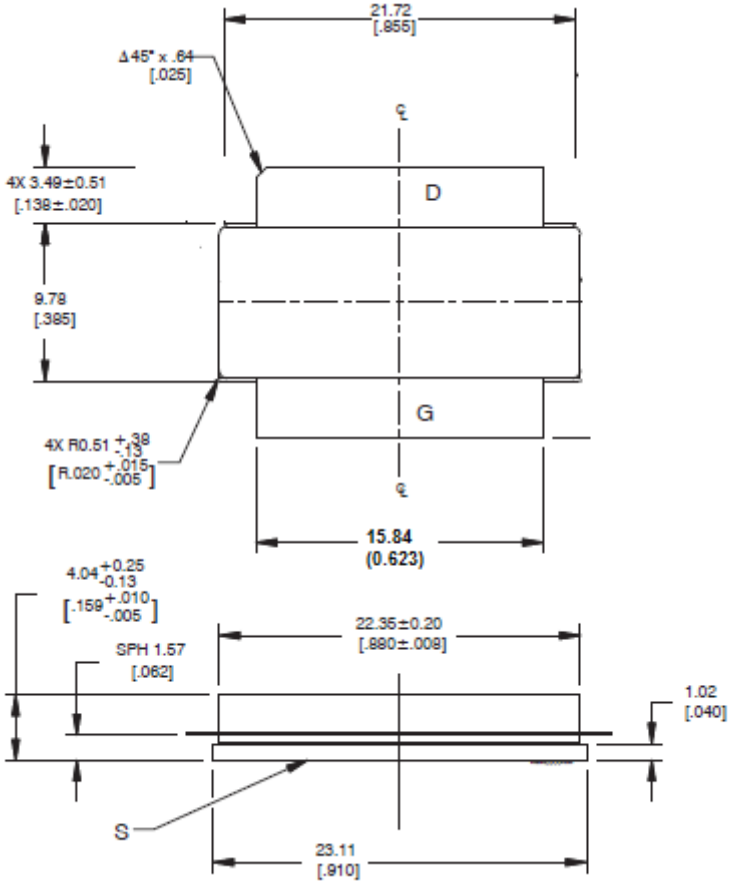


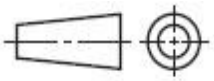
Table 5. Test Circuit Component Designations and Values

Component	Description	Suggestion
C1	8.2pF/MQ101111	
C2,C3	220pF/MQ301111	
C4,C5,C6,C9,C13,C14	10uF/1210	
C7,C8,C11,C12	10nF/1210	
C10	68pF/MQ101111	
C15,C16,C17,C19,C20,C21	390pF/MQ101111	
C18	27pF/MQ301111	/
C22	9.1pF/MQ101111	/
R1,R4	360Ω/1206	/
R2,R3	100Ω/1206	/
T1	50 Ohm,180mm	SFF-50-1.5
T2,T3	25 Ohm,180mm	SFF-25-1.5
T4,T5	12.5 Ohm,120mm	SFF-12.5-3
T6	50 Ohm,150mm	SFF-50-3
L1,L2	2.5mm wire,7turns, ϕ=5mm	DIY

Package Outline

Flangeless ceramic package;



OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-C2					09/27/2018

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2025/11/14	Rev 1.0	Advanced datasheet

Application data based on SYX-25-48

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