700MHz, 80W, 50V High Power RF LDMOS FETs

Description

The M2U0508RV is a 80-watt P1dB, highly rugged, input matched LDMOS FET, designed for wide-band commercial and industrial applications at frequencies HF to 700MHz.

It is the ruggedness and stability enhancement of M2U1508V at lower band

It can support pulsed, CW or any modulated signal in form of linear or saturated operations.



• Typical Performance (On Innogration broadband band fixtures with device soldered):

V _{ds} = 50V, V _{gs} =3.55V,I _{dq} =200mA						
Freq(MHz) Test signal Pin(dBm) Power Gain(dB) Pout(dBm) Pout(W) Eff(%					Eff(%)	
108	cw	23.5	26	49.5	90	71

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- · Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- · Pb-free, RoHS-compliant

Suitable Applications

- 2-30MHz (HF or Short wave communication)
- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 118 -140MHz (Avionics)

- 136-174MHz (Commercial ground communication)
- 160-230MHz (TV VHF III)
- 30-512MHz (Jammer, Ground/Air communication)
- 470-860MHz (TV UHF)
- 100kHz 1000MHz (ISM, instrumentation)

Table 1. Maximum Ratings

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Rating	Symbol	Value	Unit
DrainSource Voltage	V _{DSS}	125	Vdc
GateSource Voltage	V _{GS}	-10 to +10	Vdc
Operating Voltage	V _{DD}	+55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	Tc	+150	°C
Operating Junction Temperature	T₃	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case	Po IO	4.5	00/14/
T _C = 85°C, T _J =200°C, DC test	Rejc	1.5	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class	
Human Body Model (per JESD22A114)	Class 2	

Table 4. Electrical Characteristics (TA = 25 °C unless otherwise noted)

Characteristic	Symbol	Min	Тур	Max	Unit
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DC Characteristics

Drain-Source Voltage	V		125		V
V _{GS} =0, I _{DS} =1.0mA	V _{(BR)DSS}		125		V
Zero Gate Voltage Drain Leakage Current				1	^
$(V_{DS} = 50V, V_{GS} = 0 V)$	I _{DSS}	<u> </u>		ļ	μΑ
GateSource Leakage Current				1	^
$(V_{GS} = 10 \text{ V}, V_{DS} = 0 \text{ V})$	I _{GSS}			1	μΑ
Gate Threshold Voltage	V and		0.70		V
$(V_{DS} = 50V, I_D = 600 \mu A)$	V _{GS} (th)	<u>——</u>	2.73		V
Gate Quiescent Voltage	V		3.55		V
(V _{DD} = 50 V, I _D = 350-mA, Measured in Functional Test)	$V_{GS(Q)}$		3.55		V
Common Source Input Capacitance	C _{ISS}		57		pF
(V _{GS} = 0V, V _{DS} =50 V, f = 1 MHz)					
Common Source Output Capacitance	Coss		24		pF
(V _{GS} = 0V, V _{DS} =50 V, f = 1 MHz)					
Common Source Feedback Capacitance	C _{RSS}		0.75		pF
(V _{GS} = 0V, V _{DS} =50 V, f = 1 MHz)					

108MHz

TYPICAL CHARACTERISTICS



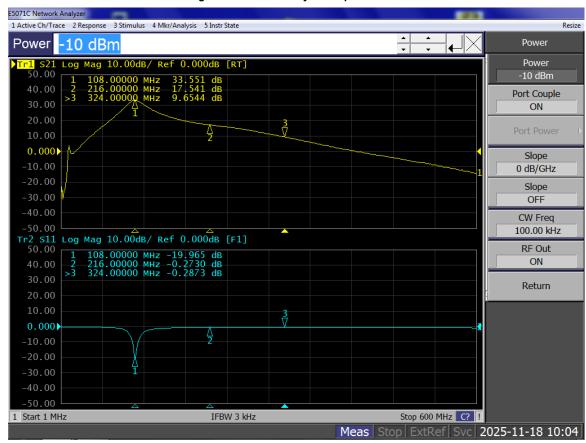
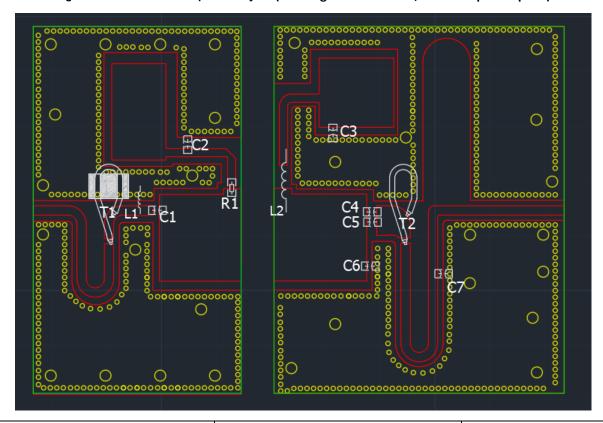
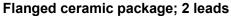


Figure 3. Test Circuit Component Layout (PCB Roger 4350B 30Mil, PCB file upon request)



Component	Description	Suggestion
C1	220pF/MQ301111	
C2,C3	10uF/1210	/
C4,C5	560pF/MQ101111	/
C6	39PF/MQ101111	
C7	2.2pF/MQ101111	
R1	360 Ω	1206
T1	25 Ohm,50mm	SFF-25-1.5/BN-61-202
T2	T2 50 Ohm,100mm	
L1	0.8mm wire,4turns, φ=3mm	DIY
L2	0.8mm wire,9turns, φ=3mm	DIY
D2	25 Ohm,25mm/FB-61-2501	SFF-25-1.5
T1	25 Ohm,31mm SFF-25-1.5	
T2	25 Ohm,24mm SFF-25-1.5	
L1	0.8mm wire,13turns, φ=3mm	DIY

Package Outline



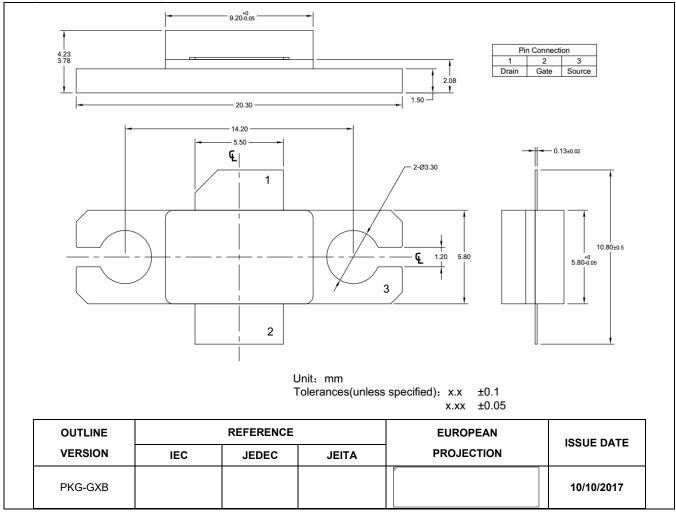


Figure 1. Package Outline PKG-G2E

Document Number: M2U0508RV Preliminary Datasheet V1.0

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2025/11/22	V1.0	Preliminary Datasheet Creation

Application data based on SYX-25-53

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