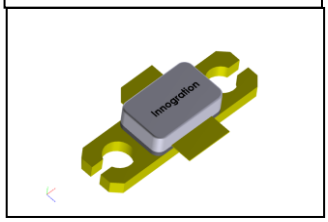
M2U0502RV LDMOS TRANSISTOR

Document Number: M2U0502RV
Preliminary Datasheet V1.0

700MHz, 20W, 50V High Power RF LDMOS FETs

M2U0502RV



Description

The M2U0502RV is a 20-watt P1dB, highly rugged, input matched LDMOS FET, designed for wide-band commercial and industrial applications at frequencies HF to 700MHz.

It is the ruggedness and stability enhancement of MU1503V at lower band， and used to replace BLF571 etc。

It can support pulsed, CW or any modulated signal in form of linear or saturated operations.

•Typical Performance (On Innogration broadband band fixtures with device soldered):

V_{ds}= 50V, V_{gs}=3.55V,I_{dq}=200mA						
Freq(MHz)	Test signal	Pin(dBm)	Power Gain(dB)	Pout(dBm)	Pout(W)	Eff(%)
108	CW	15.8	29	44.8	30	71

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- 2-30MHz (HF or Short wave communication)
- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 118 -140MHz (Avionics)
- 136-174MHz (Commercial ground communication)
- 160-230MHz (TV VHF III)
- 30-512MHz (Jammer, Ground/Air communication)
- 470-860MHz (TV UHF)
- 100kHz - 1000MHz (ISM, instrumentation)

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	125	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	$R_{\theta JC}$	2.9	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit

DC Characteristics

Drain-Source Voltage V_{GS}=0, I_{DS}=1.0mA	$V_{(BR)DSS}$		125		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate--Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600 μA)	$V_{GS(th)}$	——	2.73	——	V
Gate Quiescent Voltage (V_{DD} = 50 V, I_D = 200-mA, Measured in Functional Test)	$V_{GS(Q)}$	——	3.7	——	V
Common Source Input Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz)	C_{ISS}		22		pF
Common Source Output Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz)	C_{OSS}		9.7		pF
Common Source Feedback Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz)	C_{RSS}		0.18		pF

108MHz

TYPICAL CHARACTERISTICS

Figure 2: Network analyzer output S11/S21

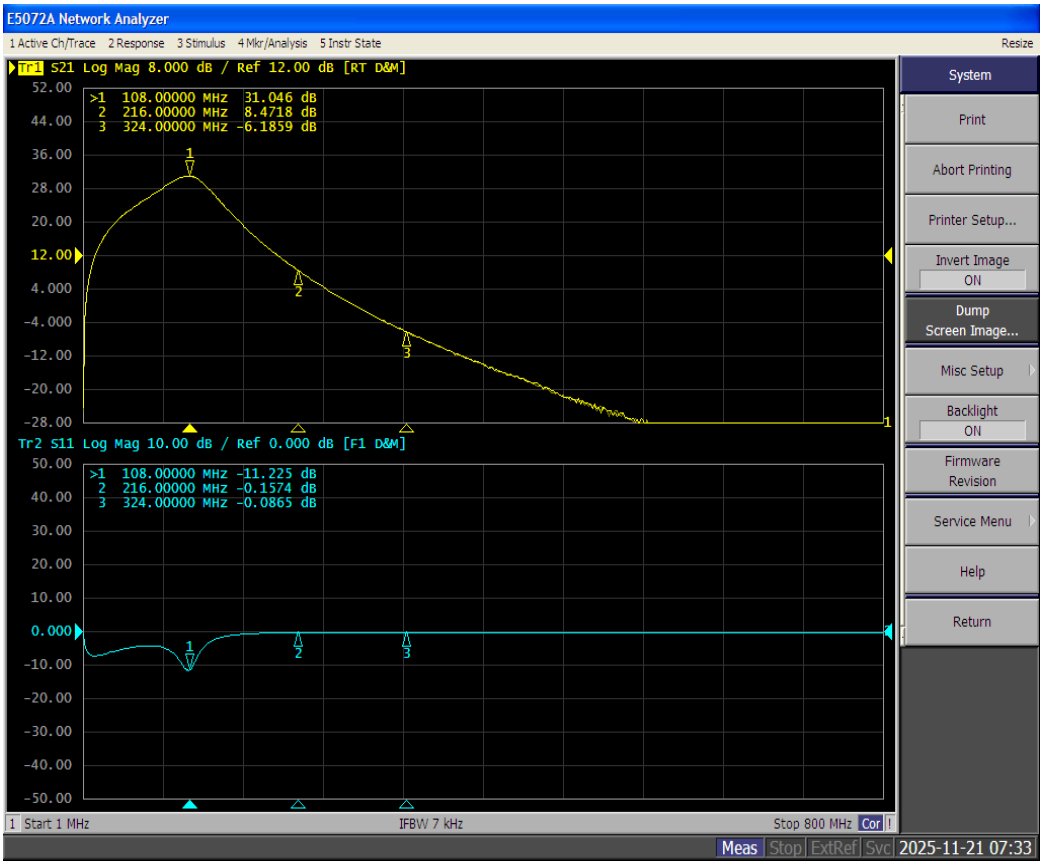
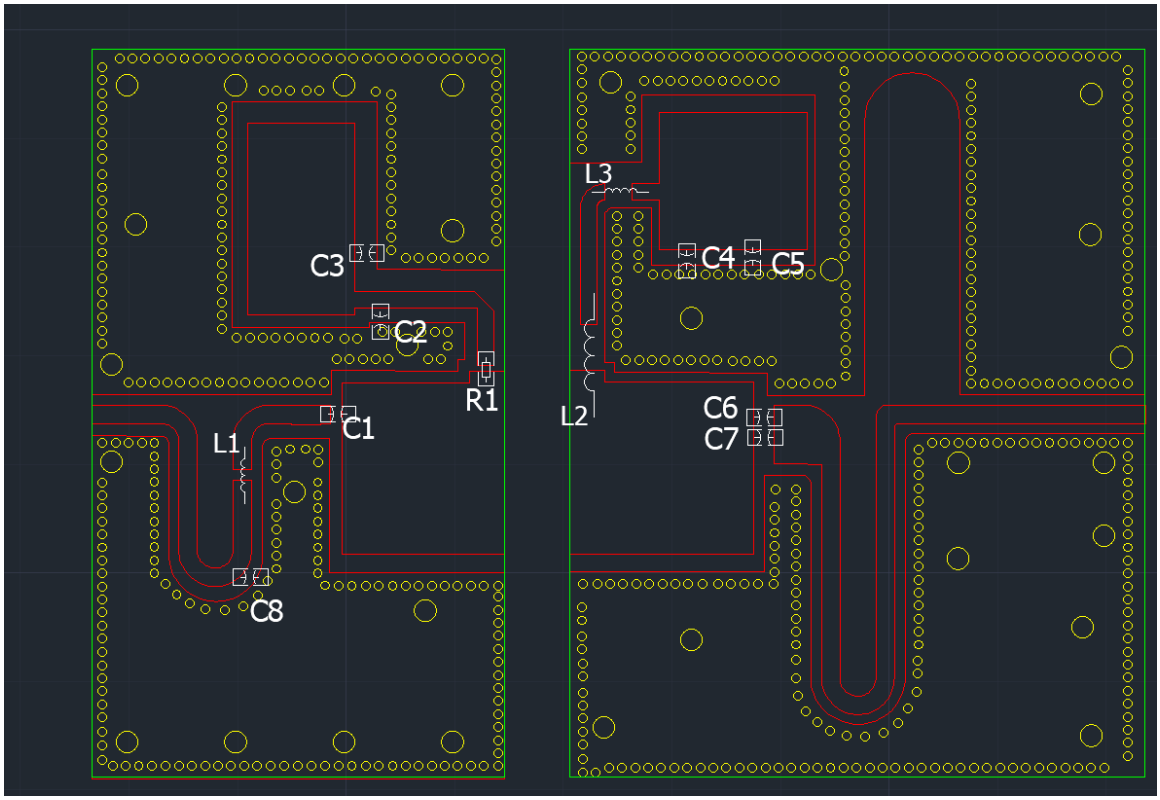


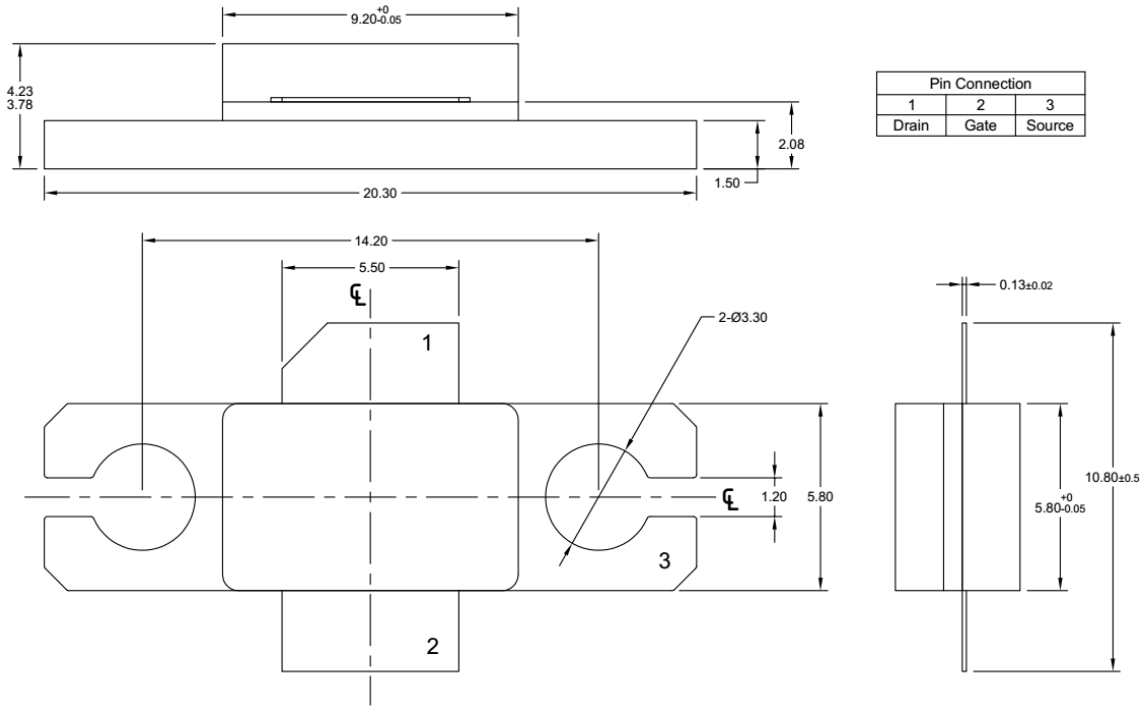
Figure 3. Test Circuit Component Layout (PCB Roger 4350B 30Mil, PCB file upon request)



Component	Description	Suggestion
C1	470pF/MQ301111	
C2,C4	10nF/1210	/
C3,C5	10uF/1210	/
C6,C7	910pF/MQ301111	
C8	39pF/MQ301111	
R1	100 Ω	1206
L1	0.8mm wire,8turns, ϕ=3mm	DIY
L2	1mm wire,2turns, ϕ=3mm	DIY
L3	1mm wire,5turns, ϕ=3mm	DIY

Package Outline

Flanged ceramic package; 2 leads



OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-GXB					10/10/2017

Figure 1. Package Outline PKG-G2E

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2025/11/22	**V1.0**	**Preliminary Datasheet Creation**

Application data based on SYX-25-54

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