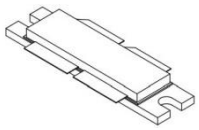
MQ012K2VPX LDMOS TRANSISTOR

Document Number: MQ012K2VPX
Preliminary Datasheet V1.0

2200W, 50V High Power RF LDMOS FETs

MQ012K2VPX



Description

The MQ012K2VPX is a 2200W capable, highly rugged, unmatched LDMOS FET, designed for commercial and industrial applications with frequencies HF to 150MHz

It is featured for industry leading high power and high ruggedness, suitable for Industrial, Scientific and Medical application, as well as HF communication, VHF TV and Aerospace applications.

- Application data at multiple frequencies

Freq(MHz)	Voltage(V)/Idq(mA)	Signal type	Pin(dBm)	Pout(W)	Power Gain(dB)	Eff(%)
108	50/200	CW	47.5	2333	16.2	82

Features

- High breakdown voltage enable possible class E operation at lower Vdd
- High Efficiency and Linear Gain Operations
- On chip RC network enable high stability and ruggedness
- Integrated ESD Protection
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Excellent thermal stability, low HCI drift
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain—Source Voltage	V_{DSS}	140	Vdc
Gate—Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case ,Case Temperature 85°C, 2000W CW, 50 Vdc, I_{DQ} = 240 mA	$R_{\theta JC}$	0.09	°C/W
Transient thermal impedance from junction to case Tj = 150° C; tp = 100 us; Duty cycle = 20 %	Zth	0.013	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22—A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage V_{GS}=0V, I_{DS}=1.0Ma	$V_{(BR)DSS}$		140		V
Zero Gate Voltage Drain Leakage Current	I_{DSS}	——	——	1	μA

(V_{DS} = 50V, V_{GS} = 0 V)					
Gate—Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600 μA)	$V_{GS(th)}$	——	2.54	——	V
Gate Quiescent Voltage (V_{DD} = 50 V, I_D = 240 Ma, Measured in Functional Test)	$V_{GS(Q)}$	——	3	——	V
Drain source on state resistance (V_{DS} = 0.1V, V_{GS} = 10 V) Each section side of device measured	Rds(on)		100		mΩ
Common Source Input Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz) Each section side of device measured	C_{ISS}		1170		pF
Common Source Output Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz) Each section side of device measured	C_{OSS}		290		pF
Common Source Feedback Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz) Each section side of device measured	C_{RSS}		7.2		pF

TYPICAL CHARACTERISTICS (108MHz)

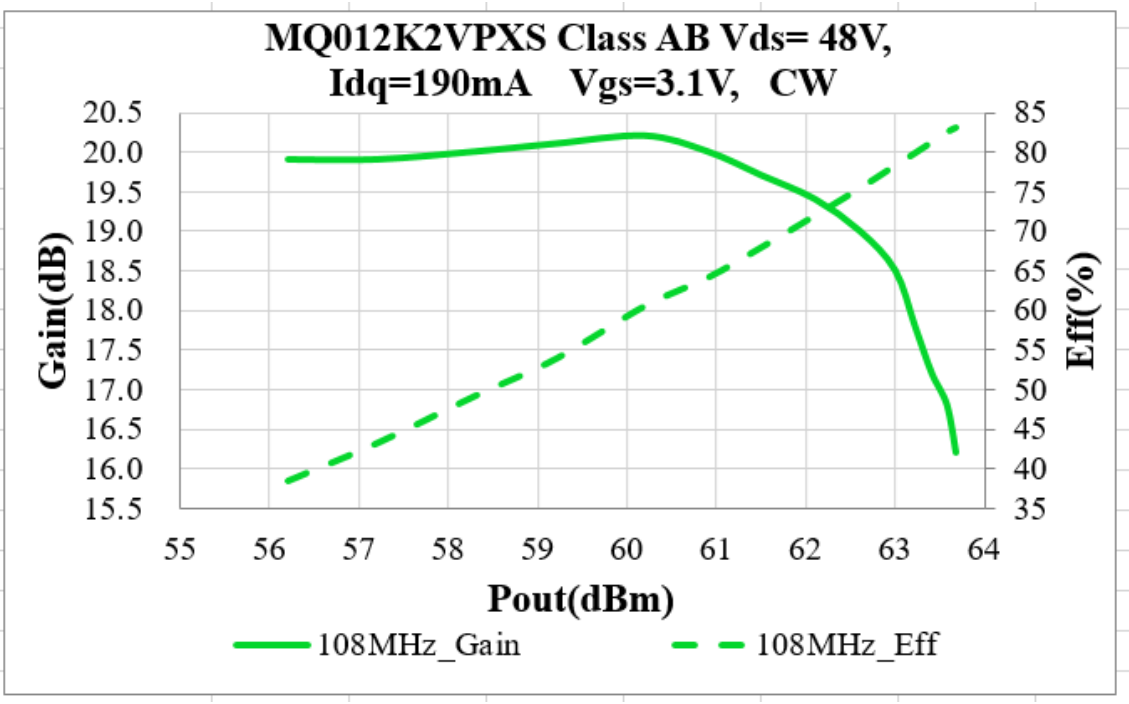


Figure 1: Efficiency and power gain as the function of Pout (Vds=50V, Idq=200mA)

Reference Circuit of Test Fixture (108MHz Power Amplifier)

Note: This demo board is used for short time demonstration only, for long time CW operation, heat management for some components might needed

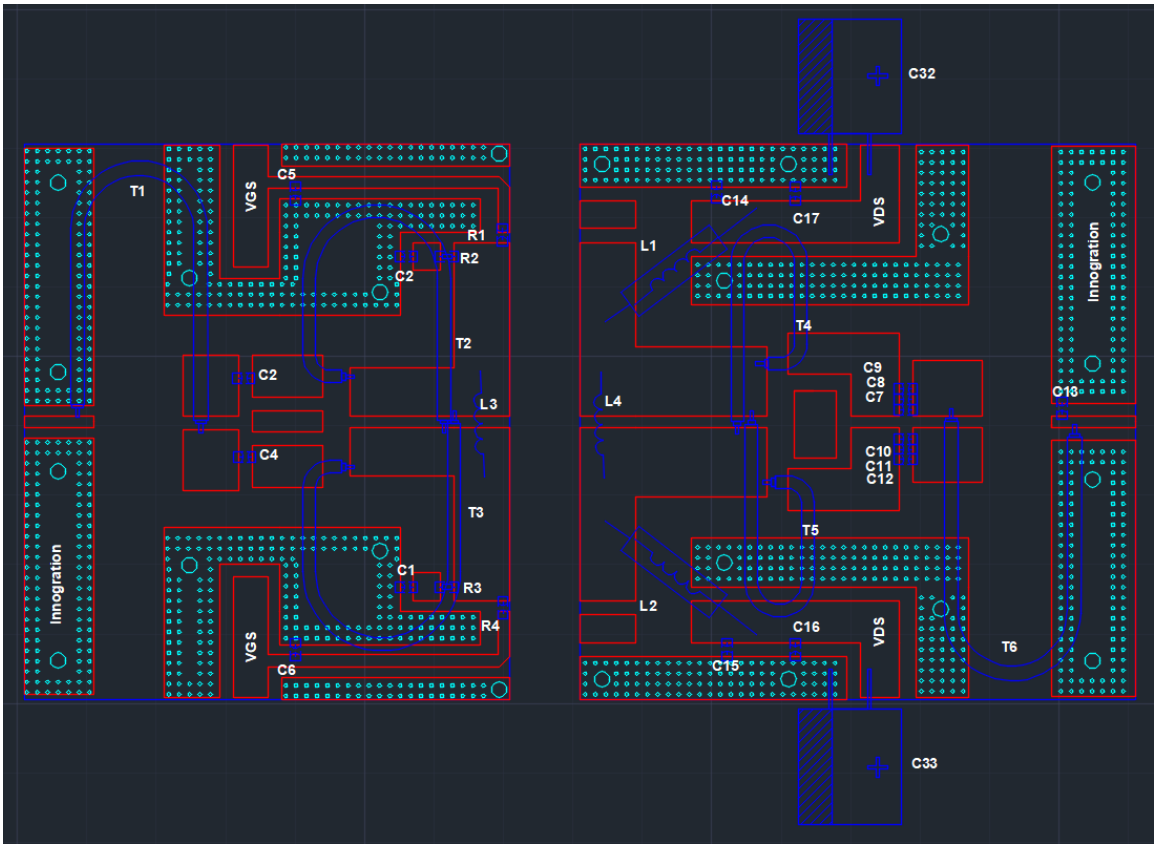
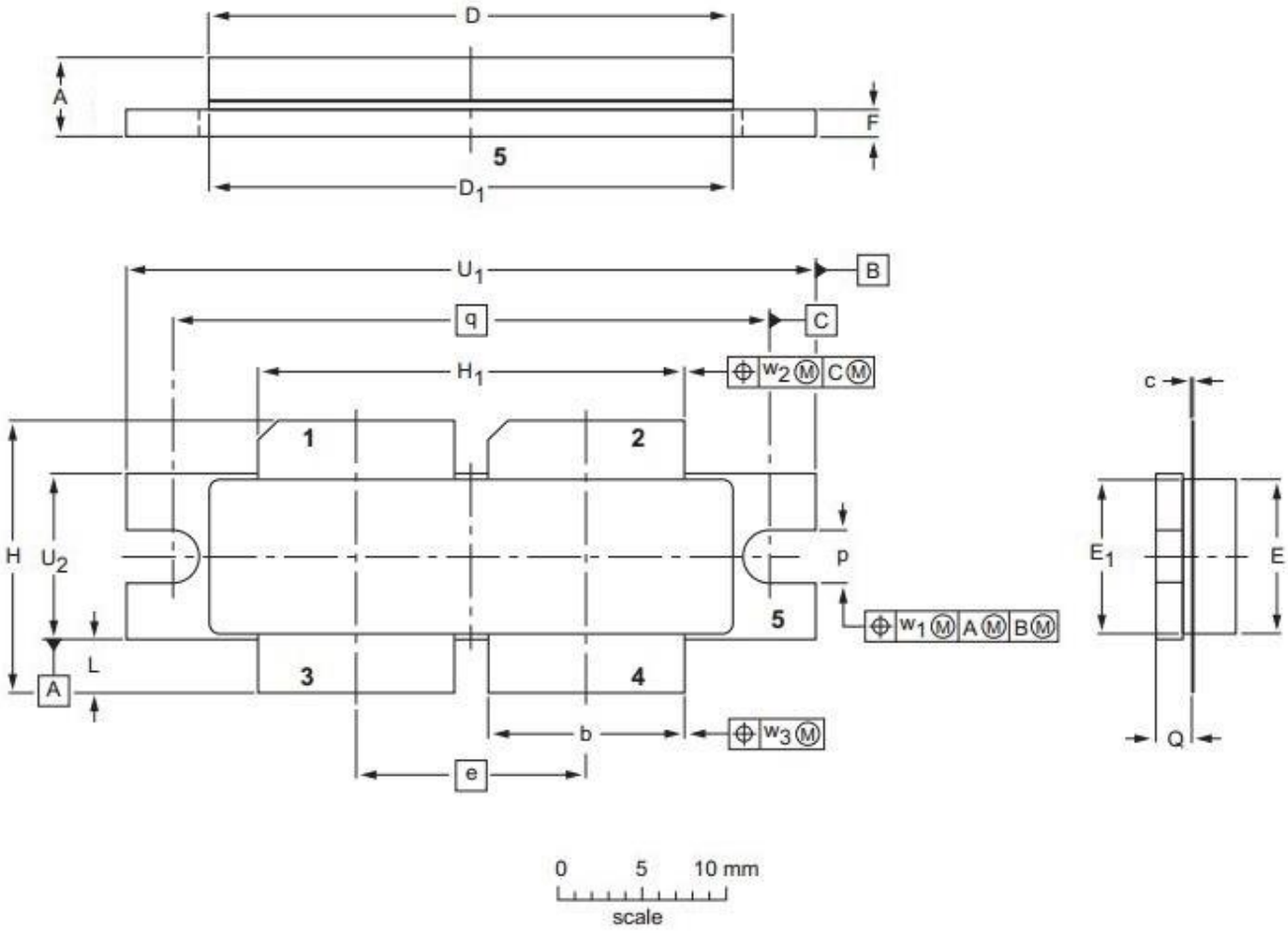


Table 5. Test Circuit Component Designations and Values

Component	Description	Suggestion
C1,C2	2.2uF / 1210	//
C5, C6, C14~C17	10uF / 1210	//
C2,C4	200pF / MQ101111	
C7~C12	560pF / MQ101111	
C13	18pF / 300V	High Efficiency tuning
	23.3 pF / 300V	High Power tuning
C32, C33	4700uF,63V	Electrolytic Capacitor
R2, R3	10Ω，1206	Chip Resistor
R1, R4	360Ω，1206	Chip Resistor
L1, L2	2mm wire ，5mm inner diameter, 6Turns	DIY
L3	0.8mm wire ，5mm inner diameter, 1.3Turns	DIY
L4	2mm wire ，3mm inner diameter, 2Turns	DIY
T1	50 ohm 200mm	SFF-50-1.5
T2, T3	25 ohm 150mm	SFF-25-1.5
T4, T5	12.5 ohm 140mm	SFF-12.5-3
T6	35 ohm 120mm	SFT-35-3
PCB	0.762mm [0.030"] thick, εr=3.50, Rogers 4350B, 1 oz. copper	

Package Outline

Flanged ceramic package; 2 mounting holes; 4 leads（1、2—DRAIN、3、4—GATE、5—SOURCE）



UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	L	p	Q	q	U_1	U_2	W_1	W_2	W_2
mm	4.7 4.2	11.81 11.56	0.18 0.10	31.55 30.94	31.52 30.96	13.72	9.50 9.30	9.53 9.27	1.75 1.50	17.12 16.10	25.53 25.27	3.48 2.97	3.30 3.05	2.26 2.01	35.56	41.28 41.02	10.29 10.03	0.25	0.51	0.25
inches	0.185 0.165	0.465 0.455	0.007 0.004	1.242 1.218	1.241 1.219	0.540	0.374 0.366	0.375 0.365	0.069 0.059	0.674 0.634	1.005 0.995	0.137 0.117	0.130 0.120	0.089 0.079	1.400	1.625 1.615	0.405 0.395	0.01	0.02	0.01

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-D4E					03/12/2013

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2025/11/25	Rev 1.0	Preliminary Datasheet

Application data based on SYX-25-52

Disclaimers