



GaN 50V, 400W, 3-4GHz RF Power Transistor

Description

The STBV38W400D4 is a dual path 400watt capable, broadband GaN HEMT, ideal for ISM and Telecom especially CW applications within full band of 3-4GHz.

In typical 3.3-3.8GHz, It can deliver 400W CW with higher effi

There is no guarantee of performance when this part is used outside of stated frequencies.

- Typical CW performance at 2.3--2.7GHz applications

$V_{DD} = 50$ Vdc, $V_{GS} = -4.1$ V, with device soldered, CW:

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff (%)	P1dB Gain (dB)	P3dB (dBm)	P3dB (W)	P3dB Eff (%)
3300	55.8	380.4	56.3	14.6	56.69	466.3	59.7
3400	56.05	402.8	55.5	13.28	56.81	479.9	58.3
3500	55.97	395.2	54.7	12.99	56.6	457.6	56.5
3600	55.85	384.8	54.8	13.32	56.48	444.5	56.3
3700	55.37	344.1	53.6	13.93	56.08	405.2	55.2
3800	55.72	373.3	53.3	12.23	56.02	401.1	53.0

Recommended driver: STAV58050J2

Applications

- S band power amplifier
- N78/N79 mobile broadband

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

Turning the device ON

1. Set VGS to the pinch-off (VP) voltage, typically -5 V
2. Turn on VDS to nominal supply voltage
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically -5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DS}	+200	Vdc
Gate--Source Voltage	V_{GS}	-8 to +0.5	Vdc
Operating Voltage	V_{DD}	55	Vdc
Maximum gate current	I_{GS}	57.6	mA
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case by FEA $T_C = 25^\circ\text{C}$, at $P_d = 400\text{W}$	$R_{\theta JC}$	0.38	°C /W

STBV38W400D4

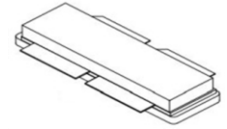




Table 3. Electrical Characteristics (TA = 25°C unless otherwise noted)

DC Characteristics (measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	VGS=-8V; IDS=57.6mA	V _{DSS}		200		V
Gate Threshold Voltage	VDS =10V, ID = 57.6mA	V _{GS(th)}	-4	-	-2	V
Gate Quiescent Voltage	VDS =50V, IDS=700mA, Measured in Functional Test	V _{GS(Q)}		-3.3		V

Ruggedness Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Load mismatch capability	3.5GHz, Pout=400W pulse CW All phase, No device damages	VSWR		10:1		

TYPICAL CHARACTERISTICS

Figure 1: Efficiency and power gain as function of Pout (V_{DD} = 50Vdc, V_{gs}=-4.1V, Pulse width=20us, duty cycle=20%)

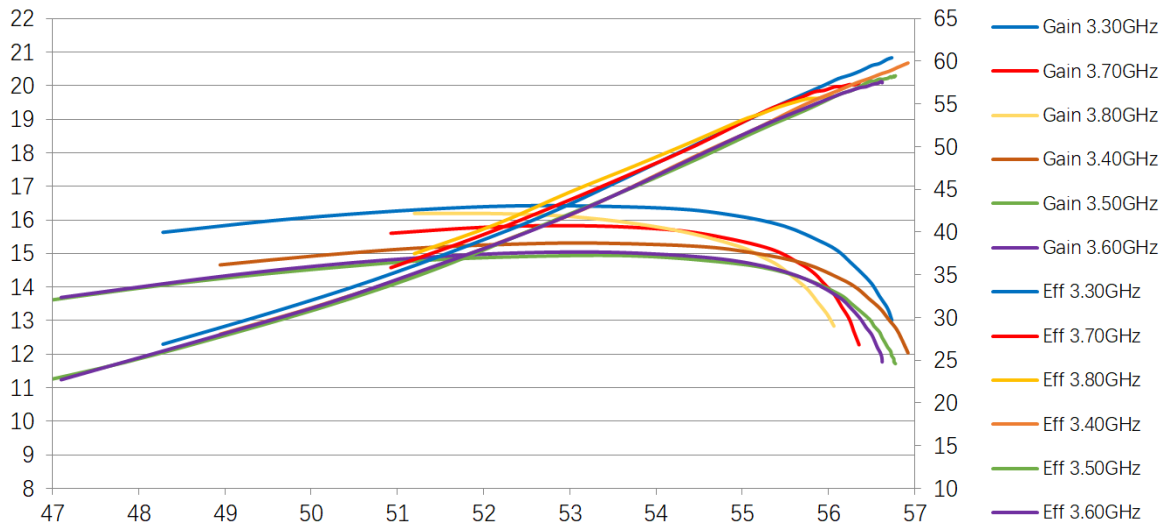
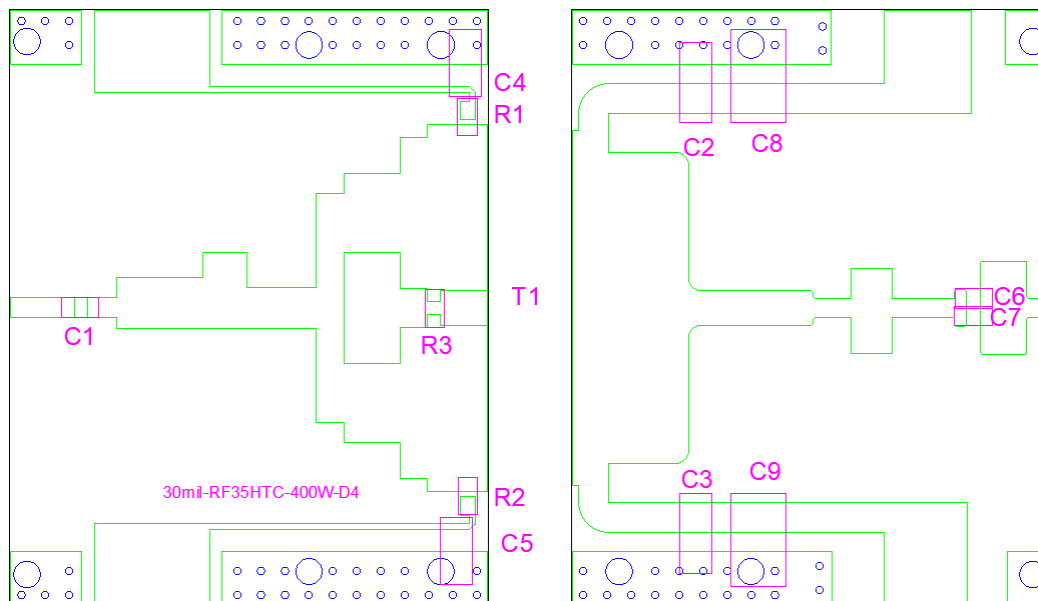


Figure 2: Network analyzer output S11/S21



Figure 2: Reference design circuit (PCB DWG file upon request,)

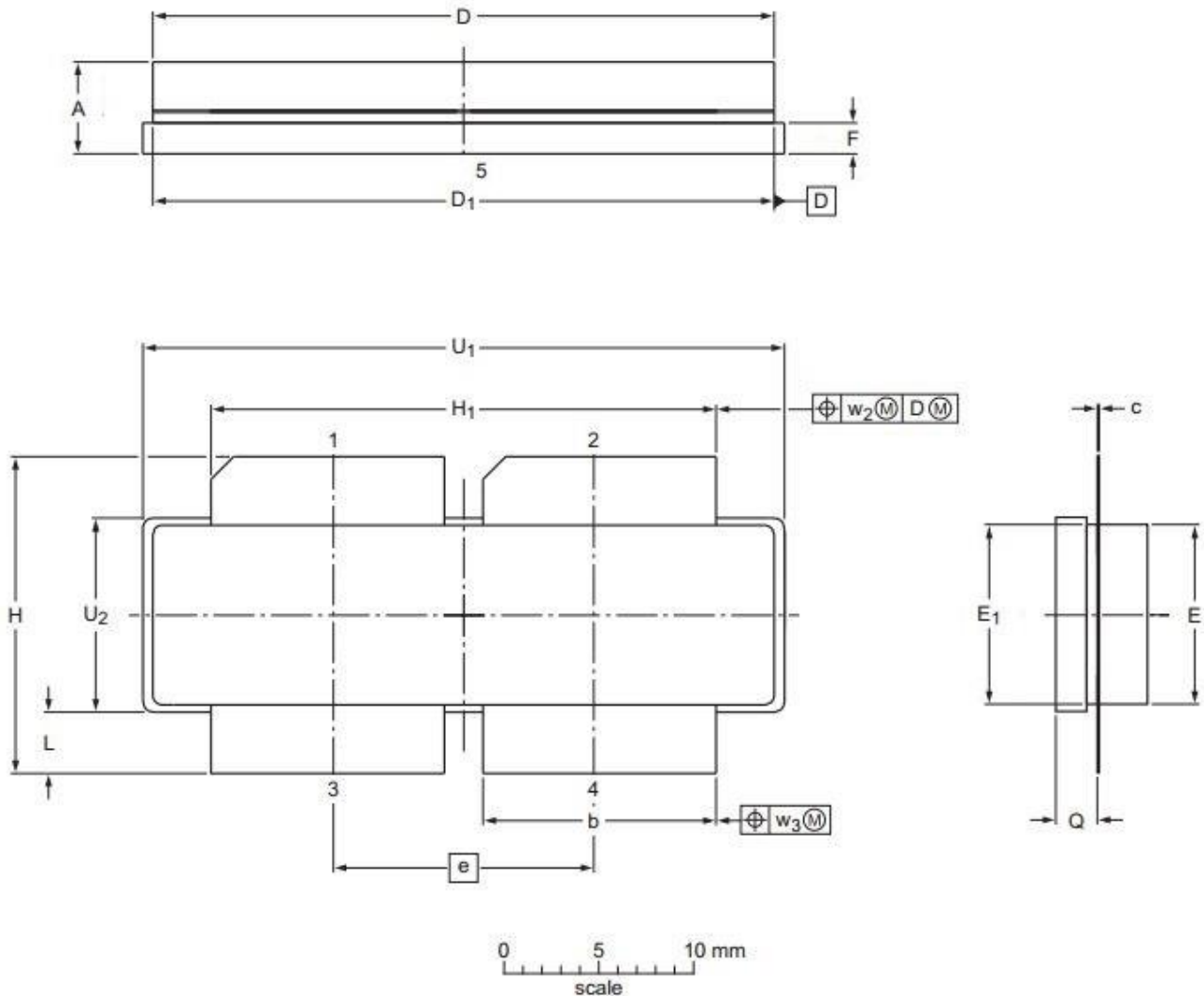


Part	Quantity	Description	Part Number	Manufacture
C1,C2,C3,C4,C5	5	8.2pF High Q Capacitor	251SHS8R2BSE	TEMEX
C6,C7	2	3.9pF High Q Capacitor	251SHF3R9BSE	TEMEX
C8,C9	2	10uF MLCC	RS80R2A106M	MARUWA
R1,R2, R3	3	10 Ω Power Resistor	ESR03EZPF100	ROHM
T1	1	400W GaN Dual Transistor	STBV38W400D4	InnogratiOn



Package Outline

Earless flanged ceramic package; 4 leads (1、2—DRAIN、3、4—GATE、5—SOURCE)



UNIT	A	b	c	D	D ₁	e	E	E ₁	F	H	H ₁	L	Q	U ₁	U ₂	W ₂	W ₂
mm	4.7	11.81	0.18	31.55	31.52	13.72	9.50	9.53	1.75	17.12	25.53	3.48	2.26	32.39	10.29	0.25	0.25
	4.2	11.56	0.10	30.94	30.96		9.30	9.27	1.50	16.10	25.27	2.97	2.01	32.13	10.03		
inches	0.185	0.465	0.007	1.242	1.241	0.540	0.374	0.375	0.069	0.674	1.005	0.137	0.089	1.275	0.405	0.01	0.01
	0.165	0.455	0.004	1.218	1.219		0.366	0.365	0.059	0.634	0.995	0.117	0.079	1.265	0.395		

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-D4					03/12/2013



Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2025/11/26	V1.0	Preliminary Datasheet Creation

Application data based on: LWH-25-42

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