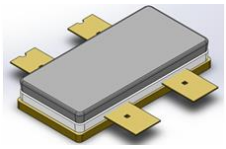
110W,12.5V High Power RF LDMOS FETs

ITGH09361RB4C



Description

The ITGH09361RB4C is a 110-watt P1dB, highly rugged, input matched LDMOS FET, designed for commercial and industrial applications at frequencies up to 520MHz. It can be used in linear or saturated power amplifier, for CW and pulsed signal, and any modulation format.

- Typical VHF CW Performance (On Innogration fixture with device soldered).

ITGH09361RB4C^{V0} VGS=2.50V VDS=12.5V Idq=400mA CW								
Freq (MHz)	**Psat (dBm)**	**Psat (W)**	**IDS (A)**	**Pin (dBm)**	**Gain (dB)**	**Eff (%)**	**2nd （dBc）**	**3rd （dBc）**
136	50.67	116.7	11.96	32.30	18.37	78.05	-20.50	-13.90
145	50.81	120.5	12.32	32.10	18.71	78.25	-21.30	-13.80
155	50.42	110.2	11.67	32.00	18.42	75.51	-24.10	-13.20
165	50.50	112.2	11.53	32.20	18.30	77.85	-25.00	-15.80
174	50.47	111.4	10.92	31.90	18.57	81.63	-27.00	-17.10

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- HF to UHF Land mobile radio (LMR)
- ISM applications

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+65	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+24	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	$R_{\theta JC}$	0.24	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage V_{GS}=0, I_{DS}=100uA	$V_{(BR)DSS}$		65		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 13.6V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate--Source Leakage Current (V_{GS} = 9 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 13.6V, I_D = 600 μA)	$V_{GS(th)}$	——	2	——	V
Gate Quiescent Voltage (V_{DD} = 13.6V, I_D = 400mA, Measured in Functional Test)	$V_{GS(Q)}$	——	2.5	——	V

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 13.6Vdc, I_{DQ} = 400 mA, f = 520 MHz

VSWR 10:1 at 110W pulse CW Output Power	No Device Degradation

136-174MHz

Reference Circuit of Test Fixture Assembly Diagram

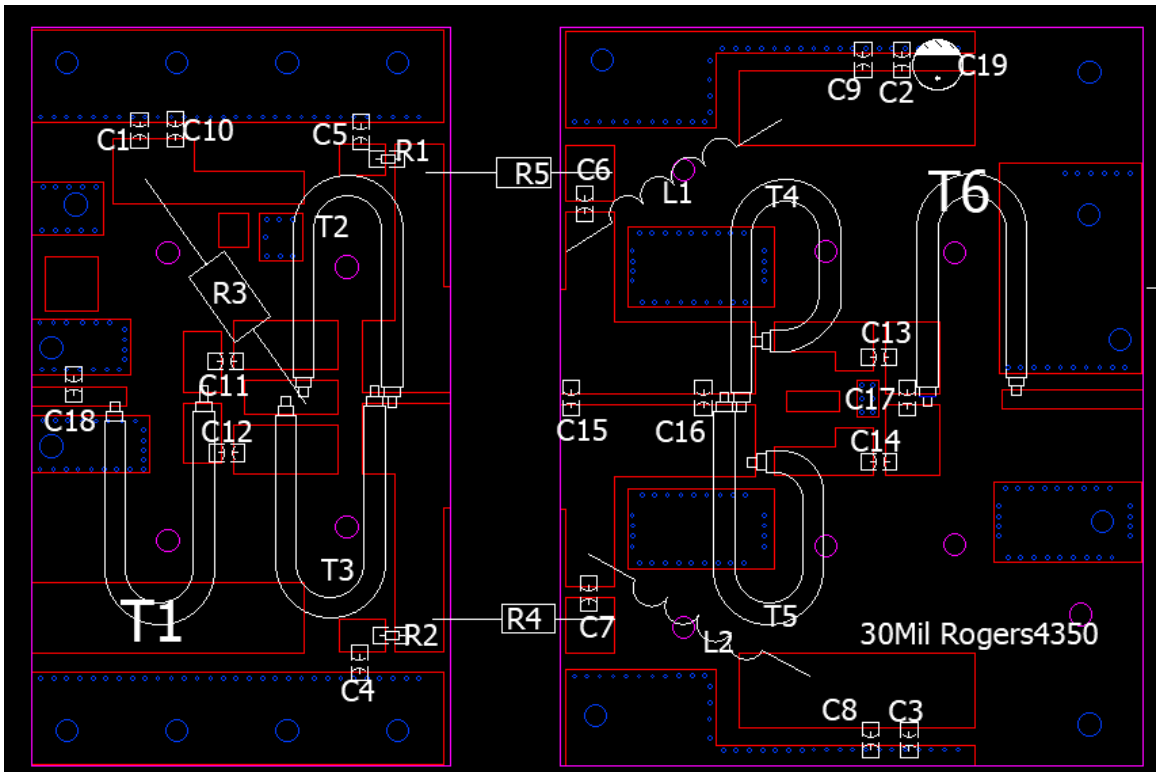
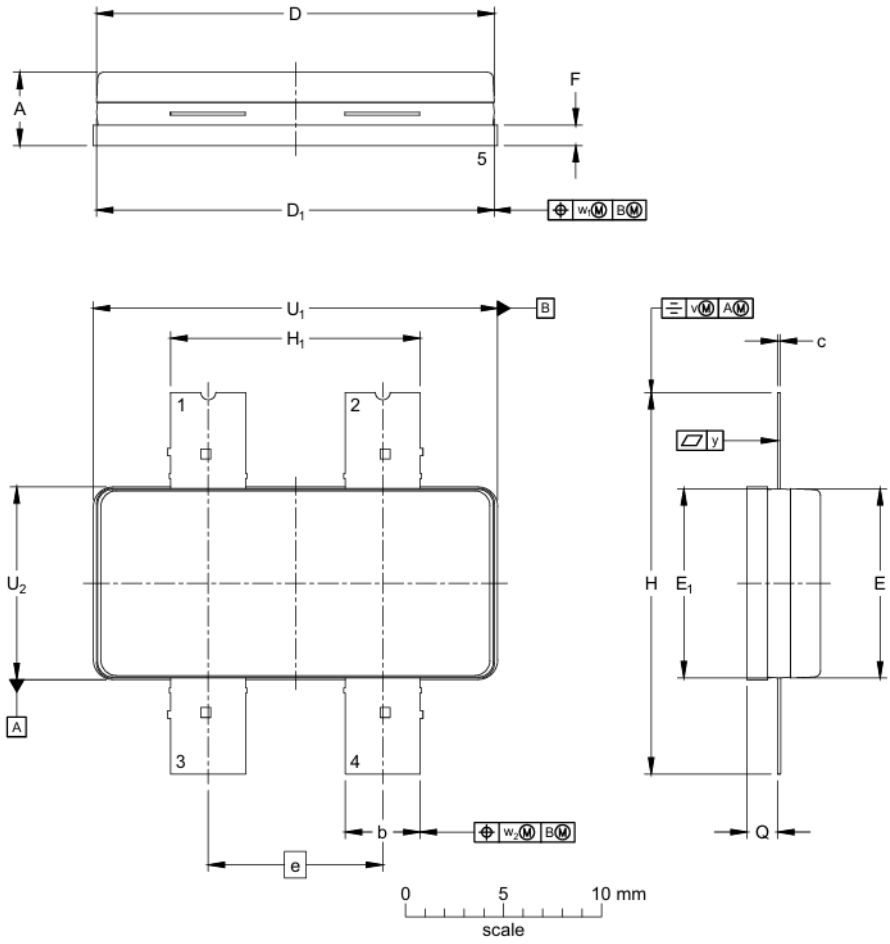


Figure 1. Test Circuit Component Layout

Table 5. Test Circuit Component Designations and Values

Component	Description	Suggestion
C1~C7	10uF/200V-1210	Ceramic multilayer capacitor
C8~10	910pF	
C11~C14	470pF	
C15	22pF	
C16	18pF	
C17	5.1pF	
C18	7.5pF	
C19	470uF/63V	electrolytic capacitor
T1	50 ohm-100mm	RFSFBU-086-50
T2,T3	16.7 ohm-100mm	SFF-16.7-1.5
T4,T5	12.5 ohm-120mm	SFF-25-1.5
T6	25 ohm-120mm	RFSFBU-086-25
R1,R2	10Ω/1206	Chip Resistor
R3	300Ω	/
R4,R5	330Ω	/
L1,L2	1.5mm wire ，5mm inner diameter， 4 Turns	DIY

Earless Flanged Plastic Air Cavity Package; 4 leads



Dimensions

Unit		A	b	c	D	D_1	E	E_1	e	F	H	H_1	Q(1)	U_1	U_2	v	w_1	w_2	y
mm	max	4.01	3.91	0.18	20.42	20.37	9.80	9.75		1.14	19.53	12.83	1.68	20.70	9.91	0.50	0.50	0.50	0.10
	nom								8.89										
	min	3.40	3.71	0.13	20.12	20.17	9.50	9.55		0.94	19.33	12.57	1.45	20.50	9.70				

Revision history

Table 7. Document revision history

Date	Revision	Datasheet Status
2025/11/12	Rev 1.0	Preliminary Datasheet

Application data based on TC-25-39

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