

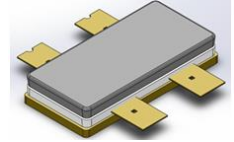


80W,12.5V High Power RF LDMOS FETs

ITGH09261RB4C

Description

The ITGH09261RB4C is a 80-watt P1dB, highly rugged, input matched LDMOS FET, designed for commercial and industrial applications at frequencies up to 520MHz. It can be used in linear or saturated power amplifier, for CW and pulsed signal, and any modulation format.



- Typical VHF CW Performance (On Innegration fixture with device soldered).

ITGH09261RB4C ^{V0} VGS=2.50V VDS=12.5V Idq=200mA CW								
Freq (MHz)	Psat (dBm)	Psat (W)	IDS (A)	Pin (dBm)	Gain (dB)	Eff (%)	2nd (dBc)	3rd (dBc)
136	50.30	107.2	12.23	35.08	15.22	70.09	-18.60	-12.10
145	50.68	116.9	13.19	35.37	15.31	70.93	-21.80	-12.00
155	50.64	115.9	13.22	35.30	15.34	70.12	-21.30	-12.10
165	50.66	116.4	13.28	35.30	15.36	70.13	-24.40	-13.40
174	50.42	110.2	11.78	34.53	15.89	74.81	-25.30	-11.80

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- HF to UHF Land mobile radio (LMR)
- ISM applications

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V _{DSS}	+65	Vdc
Gate--Source Voltage	V _{GS}	-10 to +10	Vdc
Operating Voltage	V _{DD}	+24	Vdc
Storage Temperature Range	T _{stg}	-65 to +150	°C
Case Operating Temperature	T _c	+150	°C
Operating Junction Temperature	T _J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T _C = 85°C, T _J =200°C, DC test	R _{θJC}	0.2	°C/W



Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 °C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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DC Characteristics

Drain-Source Voltage $V_{GS}=0, I_{DS}=100\mu A$	$V_{(BR)DSS}$		65		V
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 13.6V, V_{GS} = 0V$)	I_{DSS}	—	—	1	μA
Gate--Source Leakage Current ($V_{GS} = 9V, V_{DS} = 0V$)	I_{GSS}	—	—	1	μA
Gate Threshold Voltage ($V_{DS} = 13.6V, I_D = 600\mu A$)	$V_{GS(th)}$	—	2	—	V
Gate Quiescent Voltage ($V_{DD} = 13.6V, I_D = 200mA$, Measured in Functional Test)	$V_{GS(Q)}$	—	2.5	—	V

Load Mismatch (In Innegration Test Fixture, 50 ohm system): $V_{DD} = 13.6Vdc, I_{DQ} = 200mA, f = 520MHz$

VSWR 10:1 at 80W pulse CW Output Power	No Device Degradation
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136-174MHz

Reference Circuit of Test Fixture Assembly Diagram

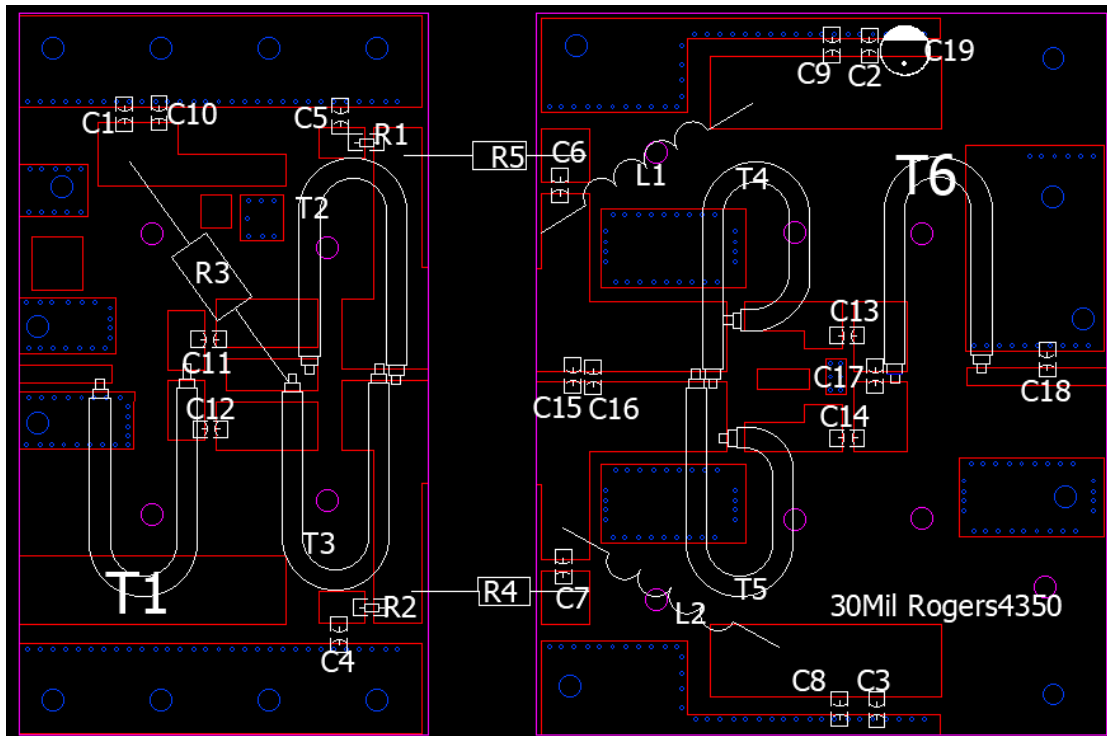


Figure 1. Test Circuit Component Layout

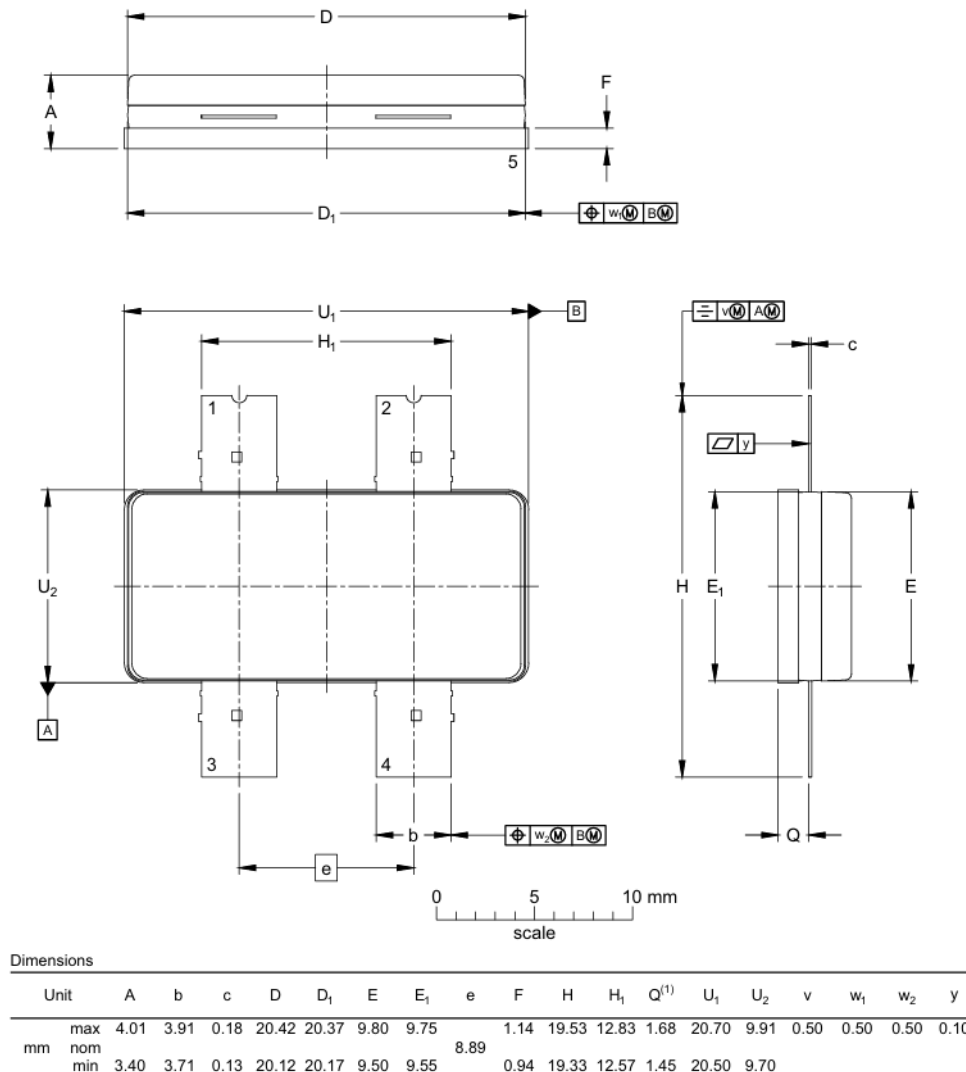


Table 5. Test Circuit Component Designations and Values

Component	Description	Suggestion
C1~C7	10uF/200V-1210	Ceramic multilayer capacitor
C8~10	910pF	
C11~C14	470pF	
C15	18pF	
C16,C17	12pF	
C18	1.5pF	
C19	470uF/63V	electrolytic capacitor
T1	50 ohm-100mm	RFSFBU-086-50
T2,T3	16.7 ohm-100mm	SFF-16.7-1.5
T4,T5	12.5 ohm-120mm	SFF-25-1.5
T6	25 ohm-120mm	RFSFBU-086-25
R1,R2	10 Ω /1206	Chip Resistor
R3	300 Ω	/
R4,R5	300 Ω	RFT-300
L1,L2	1.5mm wire , 5mm inner diameter , 4 Turns	DIY



Earless Flanged Plastic Air Cavity Package; 4 leads



Revision history

Table 7. Document revision history

Date	Revision	Datasheet Status
2025/11/3	Rev 1.0	Preliminary Datasheet

Application data based on TC-25-37

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