



## 70W,12.5V High Power RF LDMOS FETs

ITGH09240RC9

### Description

The ITGH09240RC9 is a 70-watt, highly rugged and stablied, input matched LDMOS FET, designed for commercial and industrial applications at frequencies up to 520MHz. It can be used in linear or saturated power amplifier, for CW and pulsed signal, and any modulation format.



It is also featured by its lower cost of plastic open cavity in 12\*10mm QFN package,for surface mount on PCB through high density vias or on heatsink directly

- Typical UHF CW Performance at 520M On Innegration fixture with device soldered  
 $V_{ds}=12.5V$ ,  $I_{dq}=400mA$ , ,CW

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
520	47.66	58.3	60.8	13	48.8	75	68

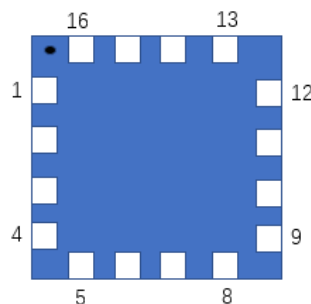
### Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

### Suitable Applications

- HF to UHF Land mobile radio (LMR)
- ISM applications

### Pin Configuration and Description (Top view)



Pin No.	Symbol	Description
5-8	RF IN/Vgs	RF Input/Gate bias
13-16	RF OUT/Vds	RF Output/Drain bias
Others	NC	Can be left as either no use or grounding
Package Base	GND	DC/RF Ground. Proposed to be soldered to heatsink plane directly for the best CW thermal and RF performance. Soldered through vias or copper coin allowed for pulsed CW applications, but will result in excessive junction temperatures and different RF performance



Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	$V_{DS}$	+65	Vdc
Gate--Source Voltage	$V_{GS}$	-10 to +10	Vdc
Operating Voltage	$V_{DD}$	+24	Vdc
Storage Temperature Range	$T_{stg}$	-65 to +150	°C
Case Operating Temperature	$T_c$	+150	°C
Operating Junction Temperature	$T_J$	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case $T_C = 85^{\circ}\text{C}$ , $T_J = 200^{\circ}\text{C}$ , DC test	$R_{\theta JC}$	0.4	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics ( $T_A = 25^{\circ}\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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## DC Characteristics

Drain-Source Voltage $V_{GS}=0$ , $I_{DS}=100\mu\text{A}$	$V_{(BR)DS}$		65		V
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 13.6\text{V}$ , $V_{GS} = 0\text{V}$ )	$I_{DSS}$	—	—	1	$\mu\text{A}$
Gate--Source Leakage Current ( $V_{GS} = 9\text{V}$ , $V_{DS} = 0\text{V}$ )	$I_{GSS}$	—	—	1	$\mu\text{A}$
Gate Threshold Voltage ( $V_{DS} = 13.6\text{V}$ , $I_D = 600\mu\text{A}$ )	$V_{GS(th)}$	—	2	—	V
Gate Quiescent Voltage ( $V_{DD} = 13.6\text{V}$ , $I_D = 400\text{mA}$ , Measured in Functional Test)	$V_{GS(Q)}$	—	2.6	—	V

Load Mismatch (In Innogrations Test Fixture, 50 ohm system):  $V_{DD} = 13.6\text{Vdc}$ ,  $I_{DQ} = 400\text{mA}$ ,  $f = 520\text{MHz}$ 

VSWR 10:1 at 70W pulse CW Output Power	No Device Degradation
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## Reference Circuit of Test Fixture Assembly Diagram 520MHz RO4350B 30mils

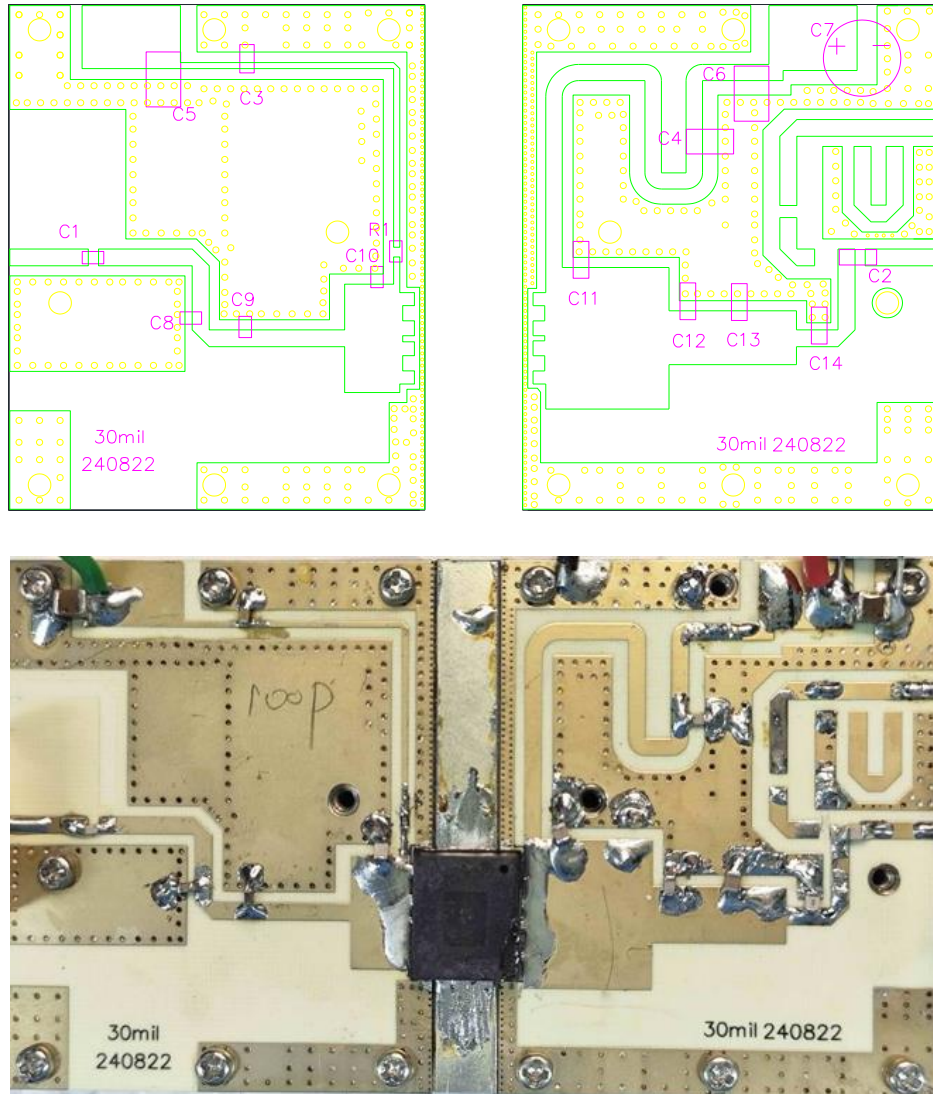
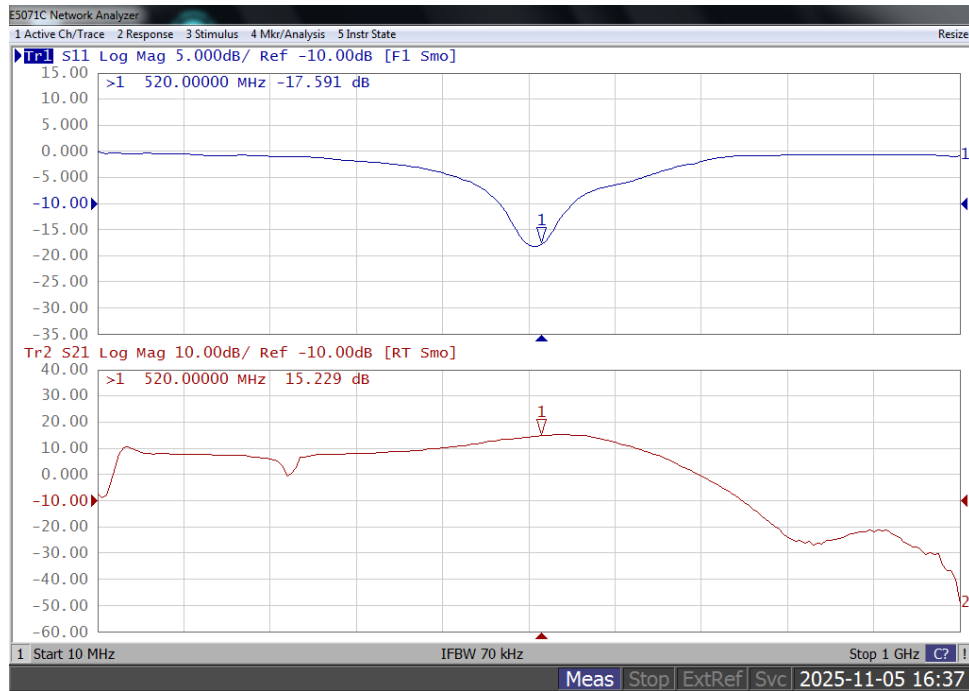


Figure 5. Test Circuit Component Layout

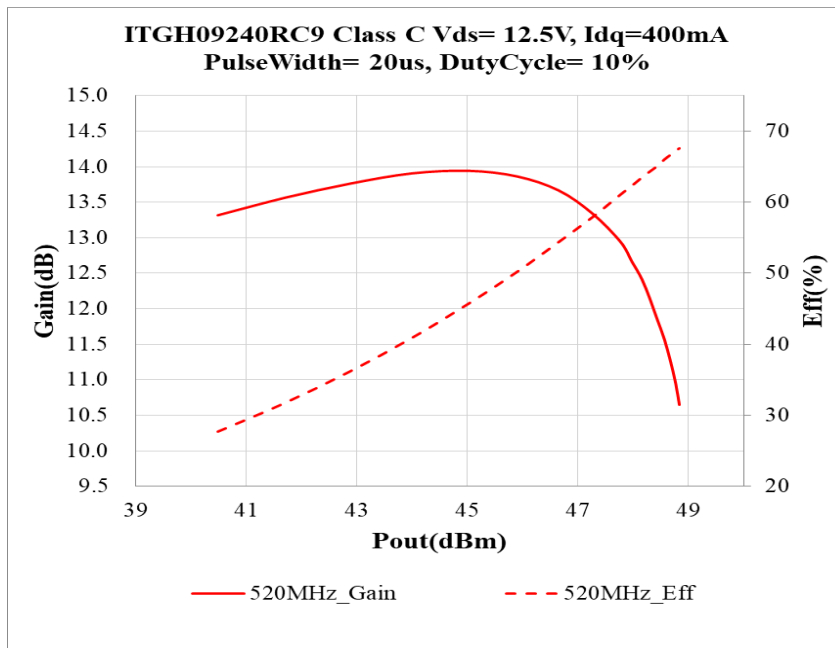
Table 5. Test Circuit Component Designations and Values

Designator	Comment	Footprint	Quantity
C1	10 pF	0805	1
C2, C3, C4	100 pF	0805	3
C5, C6	10 uF/100V	1210	2
C7	1000 uF/63V		1
C8,	3.3 pF	0805	2
C9, C11, C12, C13	20 pF	0805	4
C10	30 pF	0805	1
C14	6.8 pF	0805	1
R1	10 $\Omega$	0603	1

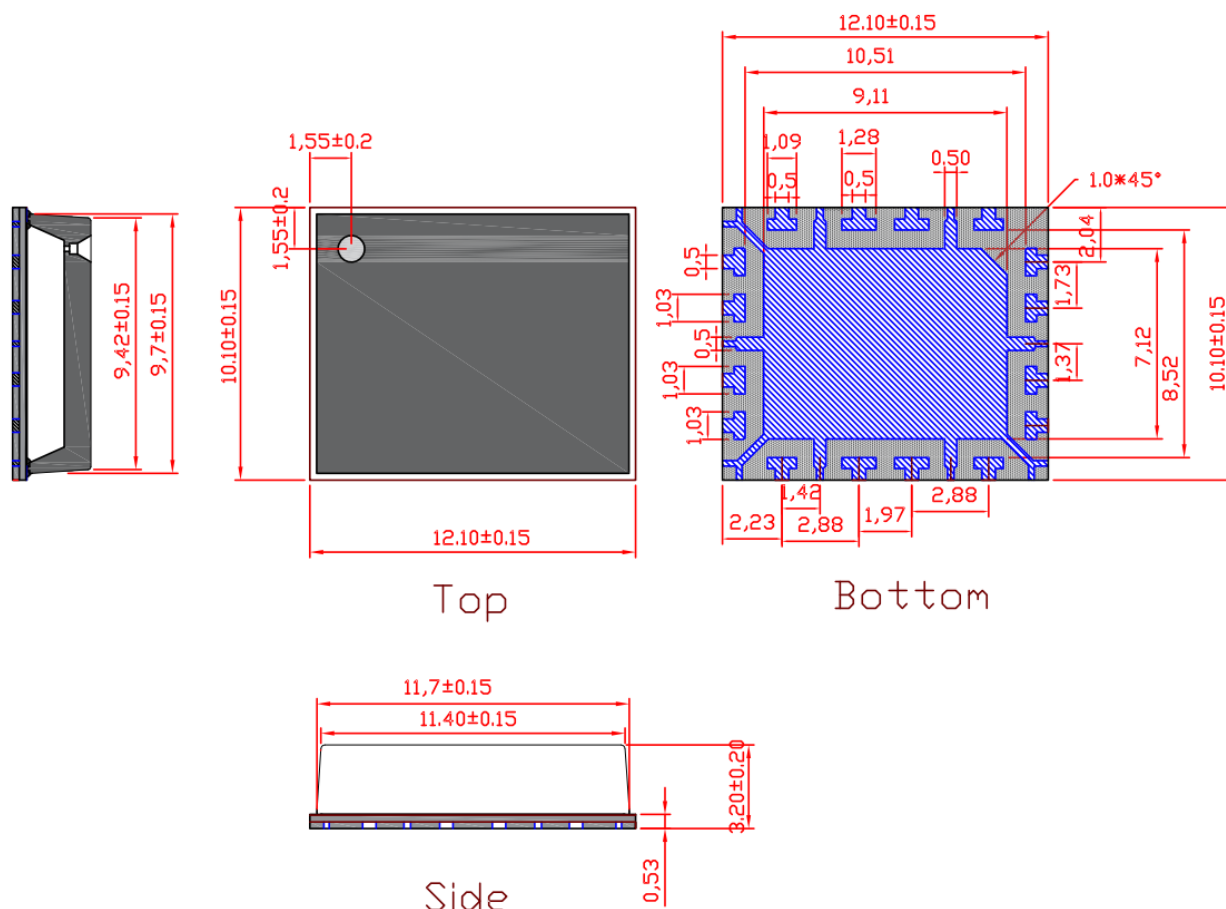
**Figure 1: Network analyzer Output S21/S11**



**Figure 2: Power gain and efficiency as function of Pout**



## Package Dimensions



## Revision history

Table 7. Document revision history

Date	Revision	Datasheet Status
2025/11/5	Rev 1.0	Preliminary Datasheet

**Application data based on LSM-25-33**

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