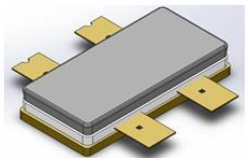
ITEV01800B4C LDMOS TRANSISTOR

Document Number: ITEV01800B4C
Product Datasheet V1.0

800W, 50V High Power RF LDMOS FETs

ITEV01800B4C



Description

The ITEV01800B4C is a 800-watt capable, high performance, unmatched LDMOS FET, designed for HF/VHF. It can be used for both CW and pulse application.

It is featured for high power and high ruggedness, low cost, suitable for ISM RF Energy application.

- Typical Performance (On Innogration 108MHz fixture with device soldered):

ITEV01800B4C VGS=3.1V VDS=50V IDQ=200mA						
Signal	Pout(dBm)	Pout(W)	Pin(dBm)	Gain(dB)	Eff(%)	2nd/3rd harmonic(dB)
Pulsed CW(10%,100us)	59.6	906	41	18.6	84	/
CW	59.3	843	41	18.3	82	-40/-21

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- On chip RC network enable high stability and ruggedness
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Excellent thermal stability, low HCI drift
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	135	Vdc
Gate--Source Voltage	V_{GS}	-7 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case ,Case Temperature 80°C, 600W CW, 50 Vdc, I_{DQ} = 200 mA	$R_{\theta JC}$	0.2	°C/W
Transient thermal impedance from junction to case Tj = 150° C; tp = 100 us; Duty cycle = 10 %	Zth	0.05	°C/W

Table 3. ESD Protection Characteristics

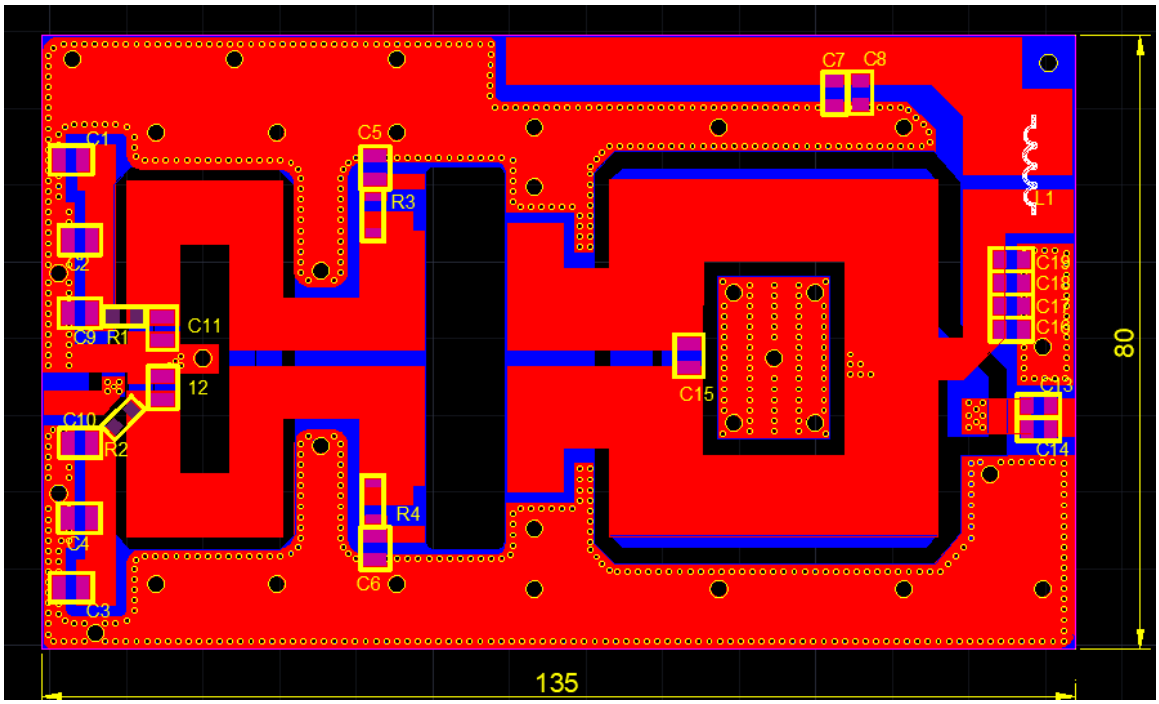
Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics (Per Side)					
Drain-Source Voltage	$V_{(BR)DSS}$		135		V

V_{GS}=0, I_{DS}=18.0mA					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50V, V_{GS} = 0 V)	I_{DSS}			1	μA
Gate—Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}			1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600 μA)	$V_{GS(th)}$		2.6		V
Gate Quiescent Voltage (V_{DD} = 50 V, I_D = 200 mA, Measured in Functional Test)	$V_{GS(Q)}$		3.36		V
Common Source Input Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz) Each section side of device measured	C_{ISS}		260		pF
Common Source Output Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz) Each section side of device measured	C_{OSS}		65		pF
Common Source Feedback Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz) Each section side of device measured	C_{RSS}		1.3		pF

Reference Circuit of Test Fixture (108MHz)

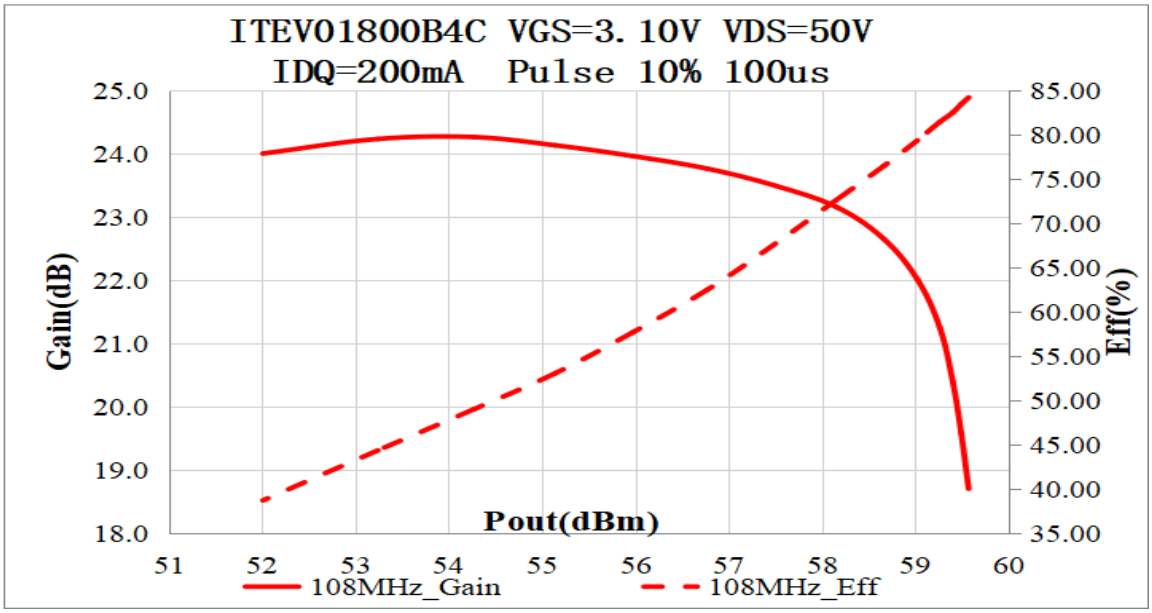


Component	Description	Suggestion
C1~C8	10uF/200V-1210	Ceramic multilayer capacitor
C9,C10	560pF	
C11,C12	510pF	
C13,C14,C16~C19	470pF	
C15	39pF	

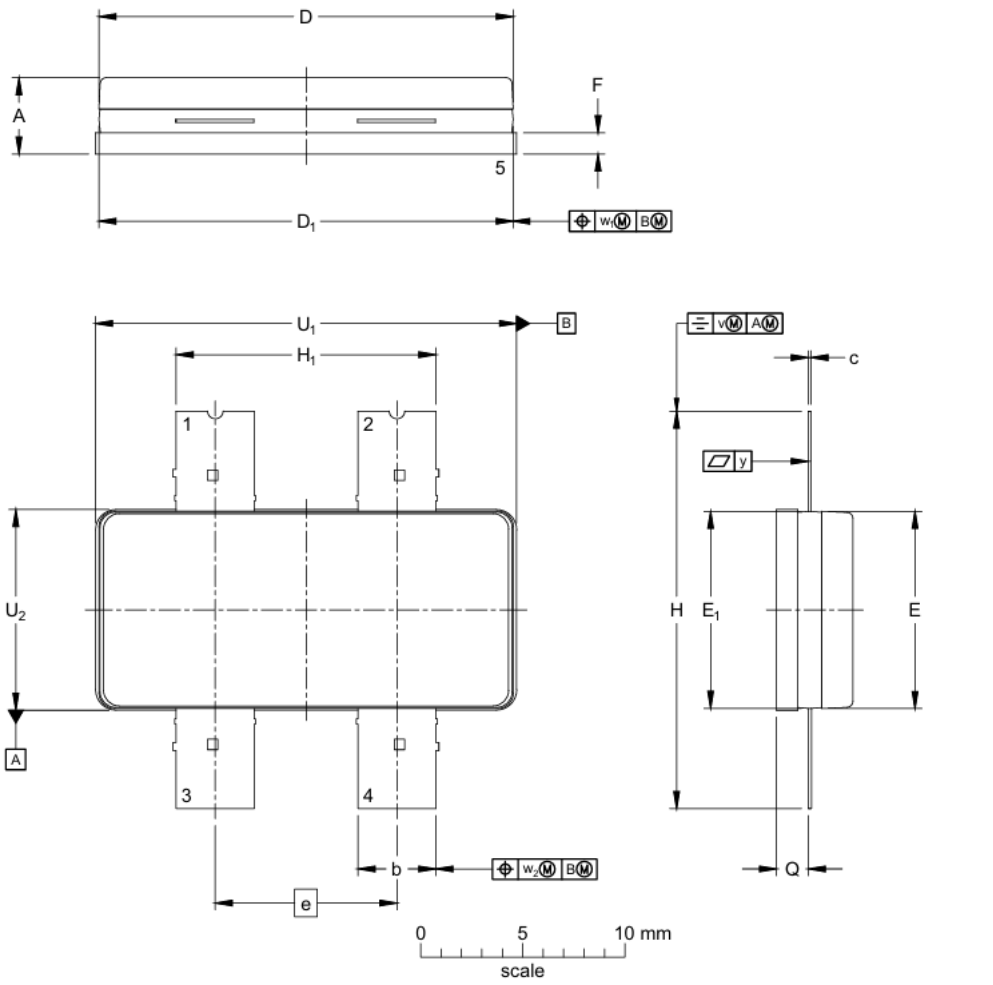
R1,R2	300Ω/1206	Chip Resistor
R3,R4	51Ω2512	Chip Resistor
L1	1.5mm wire，5mm inner diameter，7turns	DIY

Typical performance

Figure 1：Power Gain，Efficiency as function of Pout



Earless Flanged Plastic Air Cavity Package; 4 leads



Dimensions

Unit		A	b	c	D	D_1	E	E_1	e	F	H	H_1	Q(1)	U_1	U_2	v	w_1	w_2	y
mm	max	4.01	3.91	0.18	20.42	20.37	9.80	9.75		1.14	19.53	12.83	1.68	20.70	9.91	0.50	0.50	0.50	0.10
	nom								8.89										
	min	3.40	3.71	0.13	20.12	20.17	9.50	9.55		0.94	19.33	12.57	1.45	20.50	9.70				

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2025/11/7	**Rev 1.0**	**Preliminary Datasheet**

Application data based on TC-25-38

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