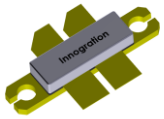
SX2054RVP GaN TRANSISTOR

Document Number: SX2054RVP
Preliminary Datasheet V1.0

Gallium Nitride 50V, 540W, RF Power Transistor

SX2054RVP



Description

The SX2054RVP is a 540-watt, unmatched GaN HEMT in form of push-pull configuration, designed for general purposes and wide band amplifier applications with frequencies from HF to 2GHz. There is no guarantee of performance when this part is used in applications designed outside of these frequencies.

•Typical Performance (On Innogration broadband application board):

I_{DQ} = 500 mA, CW

Freq(MHz)	Drain Voltage(V)	Psat(W)	Gain(dB)	Eff(%)
400-680	48	450-550	>17	65~75

Applications and Features

- Suitable for wireless communication infrastructure, wideband amplifier, EMC testing, ISM etc.
- High Efficiency and Linear Gain Operations
- Thermally Enhanced Industry Standard Package
- High Reliability Metallization Process
- Excellent thermal Stability and Excellent Ruggedness
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

Turning the device ON

1. Set VGS to the pinch--off (VP) voltage, typically –5 V
2. Turn on VDS to nominal supply voltage (50V)
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically –5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+200	Vdc
Gate--Source Voltage	V_{GS}	-8 to 0	Vdc
Operating Voltage	V_{DD}	0 to 55	Vdc
Maximum forward gate current	Igf	67.2	mA
Storage Temperature Range	Tstg	-65 to +150	C
Case Operating Temperature	T_C	-55 to +150	C
Operating Junction Temperature	T_J	+225	C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC Power Dissipation, FEA	$R_{\theta JC}$	0.45	C/W

Table 3. Electrical Characteristics (T_C = 25℃ unless otherwise noted)

DC Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V_{GS}=-8V; I_{DS}=67.2mA	V_{DSS}		200		V
Gate Threshold Voltage	V_{DS} = 10V, I_D = 67.2mA	V_{GS}(th)	-4	-	-3	V
Gate Quiescent Voltage	V_{DS} =50V, I_{DS}=500mA, Measured in Functional Test	$V_{GS(Q)}$		-3.33		V

400-678MHz

Figure 2. Network analyzer output S11/S21 VDS=48V IDQ=300mA

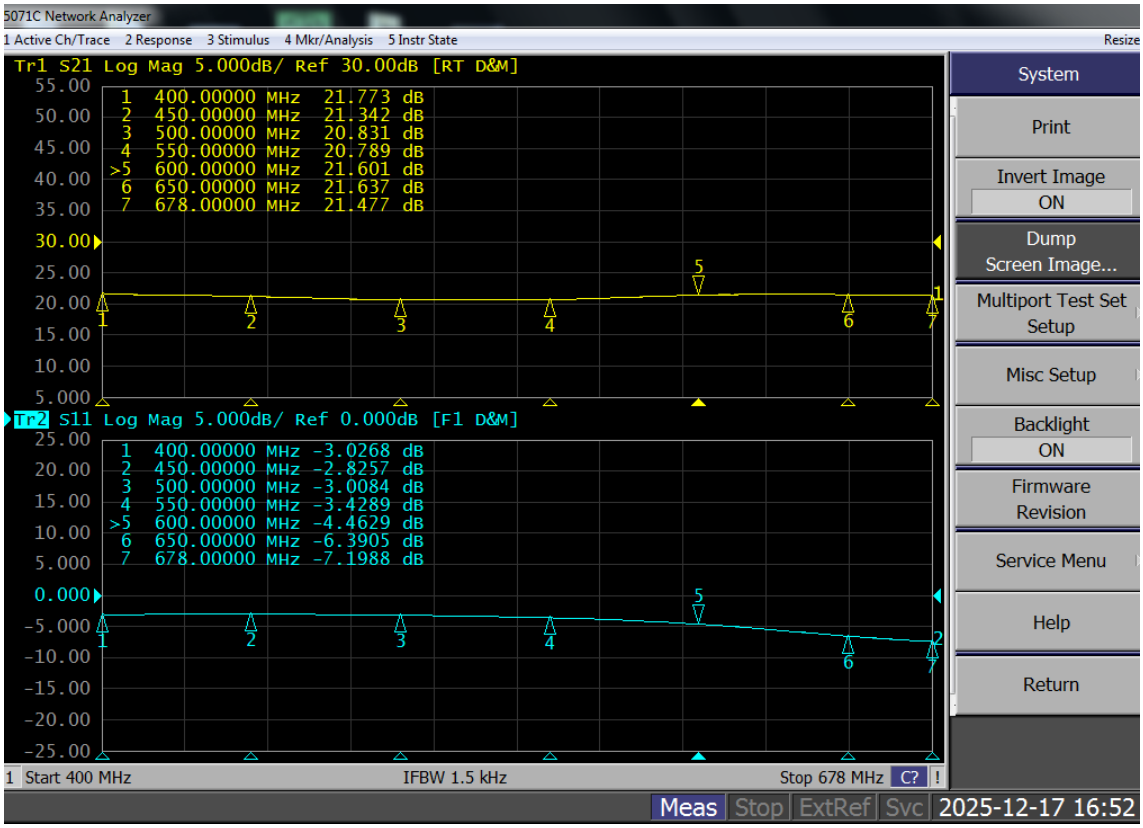


Figure 3. Test Circuit Component Layout

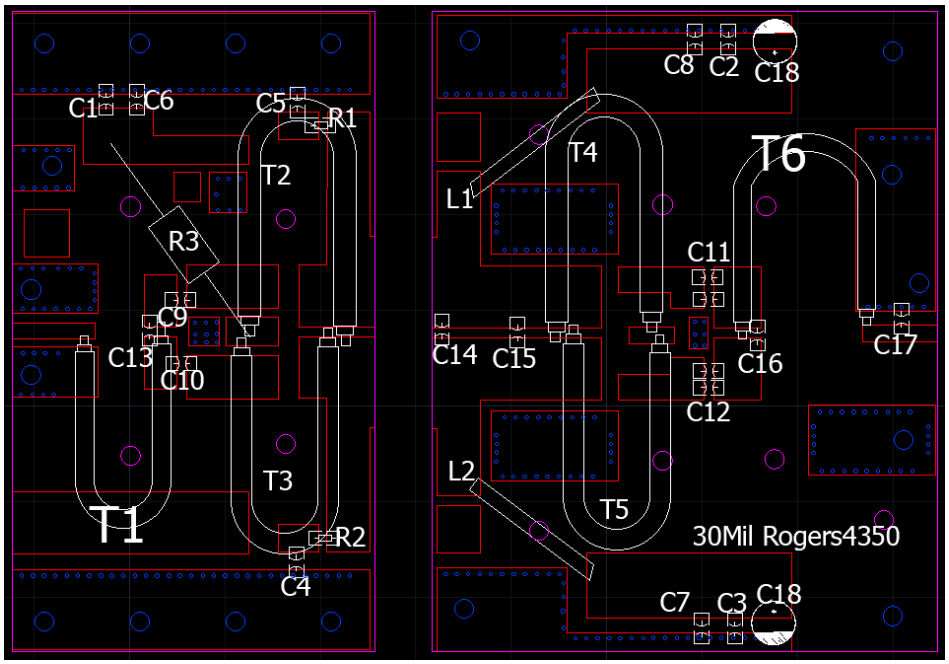
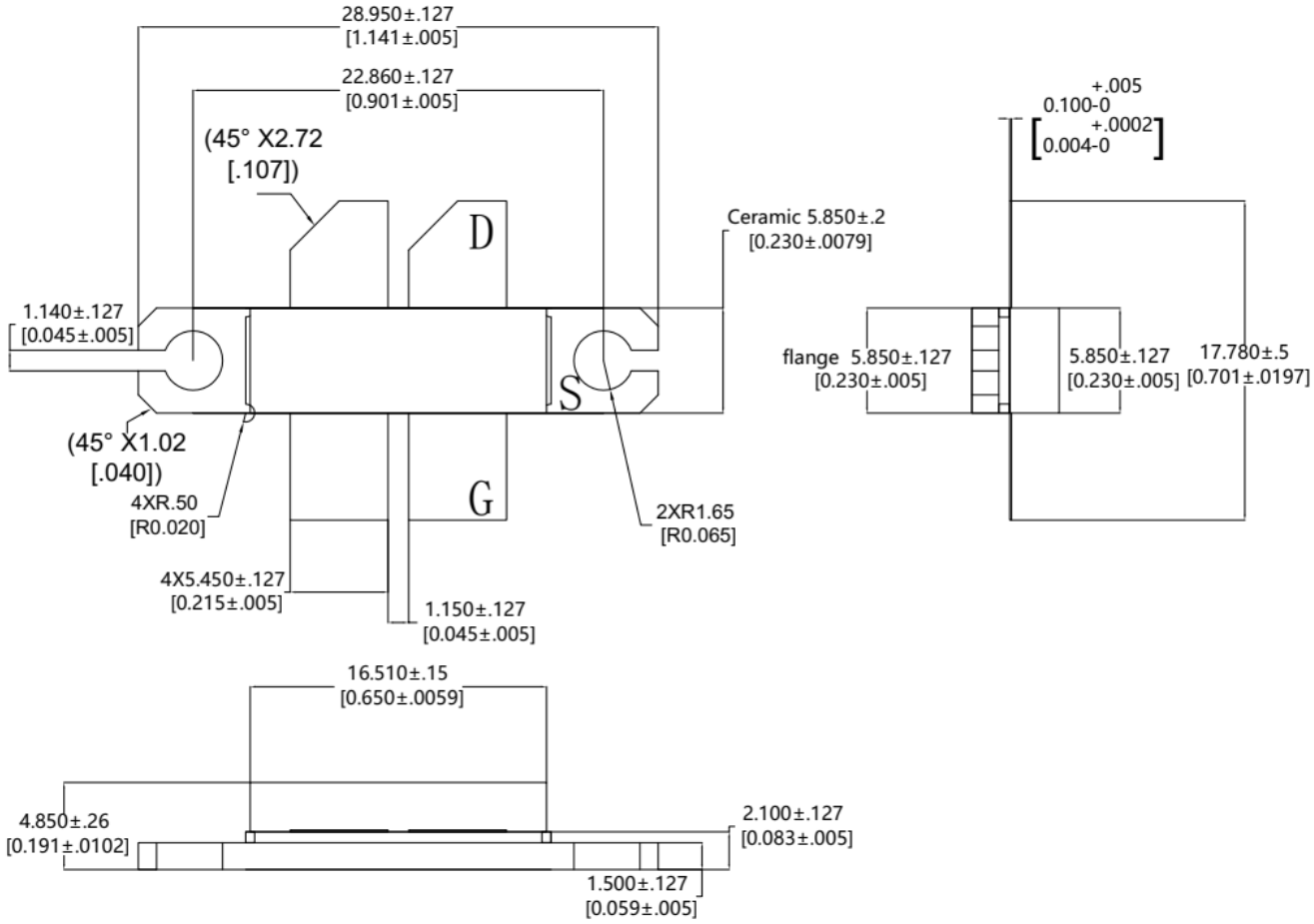


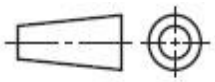
Table 4. Test Circuit Component Designations and Values

Component	Description	Suggestion
C1~C5	10uF/200V-1812	Ceramic multilayer capacitor
C6~C8	820pF	
C9,C10	30pF	
C11,C12	20pF*2	
C14	4.7pF	
C15	5.6pF	
C16	0.8pF	
C17	0.3pF	
C18	2000uF/63V	Electrolytic Capacitor
R1,R2	10Ω-1206	Chip Resistor
R3	50Ω	color ring resistor
L1	1.5mm wire	DIY
T1	50 ohm-50mm	RFSFU-086-50
T2~T5	25 ohm-40mm	RFSFU-086-25
T6	50 ohm-60mm	SFF-50-3
PCB	Rogers 4350B;30Mil	

Package Outline

Flanged ceramic package; 2 mounting holes; 4 leads



OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-LB/LBB					05/21/2021

Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2025/12/18	Rev 1.0	Preliminary Datasheet

Application data based on TC-25-45

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