



GaN HEMT 50V, 350W, 1.5-2.7GHz RF Power Transistor

Description

The STBV27W350RC2 is a 350W, single ended GaN HEMT, designed for multiple applications with Frequencies up to 3GHz. It is optimized thermally to better support wideband CW or wider pulse or higher duty cycle application. **In typical broadband application within 1.8-2.7GHz, it can deliver 300W CW**

There is no guarantee of performance when this part is used in applications designed outside of these frequencies.

STBV27W350RC2



- Typical RF performance on 1.8-2.7GHz wideband application board with device soldered

CW $V_{DS}=48V$ $I_{DQ}=100mA$

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
1800	55.13	326.2	50.3	13.05	55.59	362.4	52.6
1850	55.34	342.2	55.6	13.64	55.86	385.6	58.1
1900	55.46	351.9	59.1	14.93	56.12	409.1	62.5
2000	55.1	323.8	57.5	15.14	56.00	397.8	62.2
2100	54.24	265.4	49.2	15.47	55.66	367.8	55.7
2200	53.6	229.2	44.3	15.69	55.5	354.9	52.3
2300	53.69	233.6	44.1	14.64	55.42	348.2	50.8
2400	53.76	237.8	44.4	14.22	55.35	343.1	50.4
2500	53.86	243.2	46.6	14.98	55.41	347.2	52.9
2600	53.65	231.5	46.7	14.72	55.18	329.3	53.3
2700	53.09	203.8	45.4	14.21	54.75	302.0	51.4

Applications

- L band power amplifier application
- S band power amplifier application

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

Turning the device ON

- Set VGS to the pinch-off (VP) voltage, typically -5 V
- Turn on VDS to nominal supply voltage
- Increase VGS until IDS current is attained
- Apply RF input power to desired level

Turning the device OFF

- Turn RF power off
- Reduce VGS down to VP, typically -5 V
- Reduce VDS down to 0 V
- Turn off VGS

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	+200	Vdc
Gate-Source Voltage	V_{GS}	-8 to +0.5	Vdc
Operating Voltage	V_{DD}	55	Vdc
Maximum gate current	I_{GS}	43.2	mA
Storage Temperature Range	T_{STG}	-65 to +150	°C
Case Operating Temperature	T_c	+150	°C
Operating Junction Temperature	T_j	+225	°C



Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case by FEA $T_c = 85^\circ\text{C}$, at $P_d = 150\text{W}$,	$R_{\theta\text{JC}}$	0.55	$^\circ\text{C}/\text{W}$

Table 3. Electrical Characteristics (TA = 25°C unless otherwise noted)

DC Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS} = -8\text{V}$; $IDS = 43.2\text{mA}$	V_{DSS}		200		V
Gate Threshold Voltage	$V_{DS} = 10\text{V}$, $ID = 43.2\text{mA}$	$V_{GS(\text{th})}$	-4		-2	V
Gate Quiescent Voltage	$V_{DS} = 50\text{V}$, $IDS = 500\text{mA}$, Measured in Functional Test	$V_{GS(Q)}$		-3.3		V

Ruggedness Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Load mismatch capability	50V 2GHz, $P_{out} = 350\text{W}$ pulsed CW, All phase, No device damages	VSWR		10:1		

1.8-2.7GHz

Figure 1. Network Analyzer result S11 and S21 VDS= 50V, IDQ = 500mA

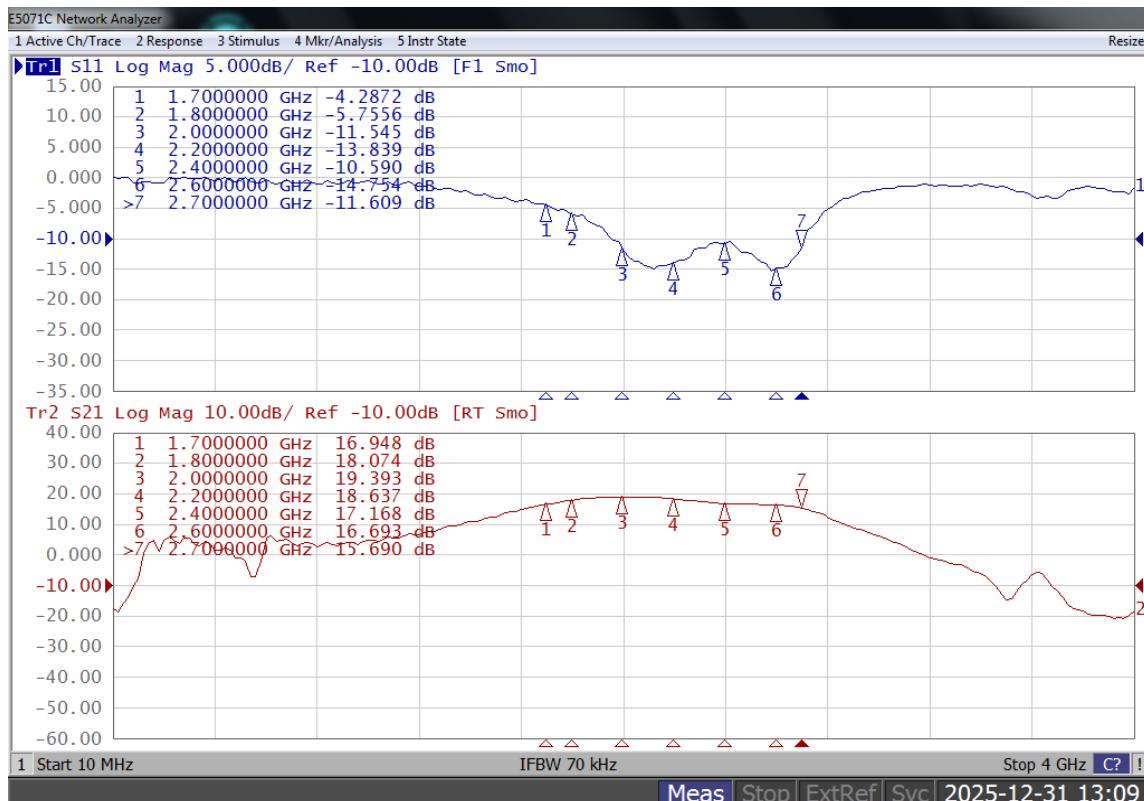


Figure 2: Picture of application board

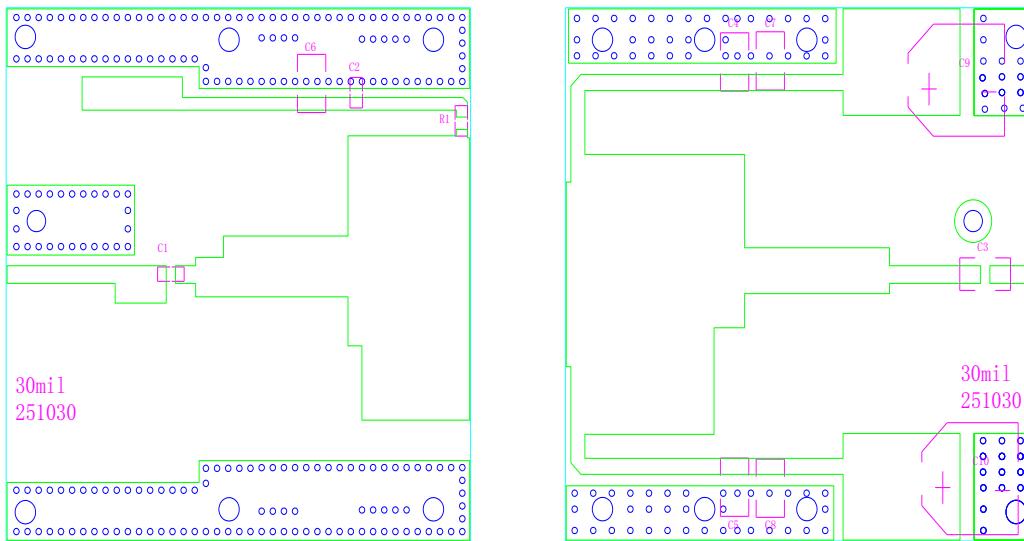


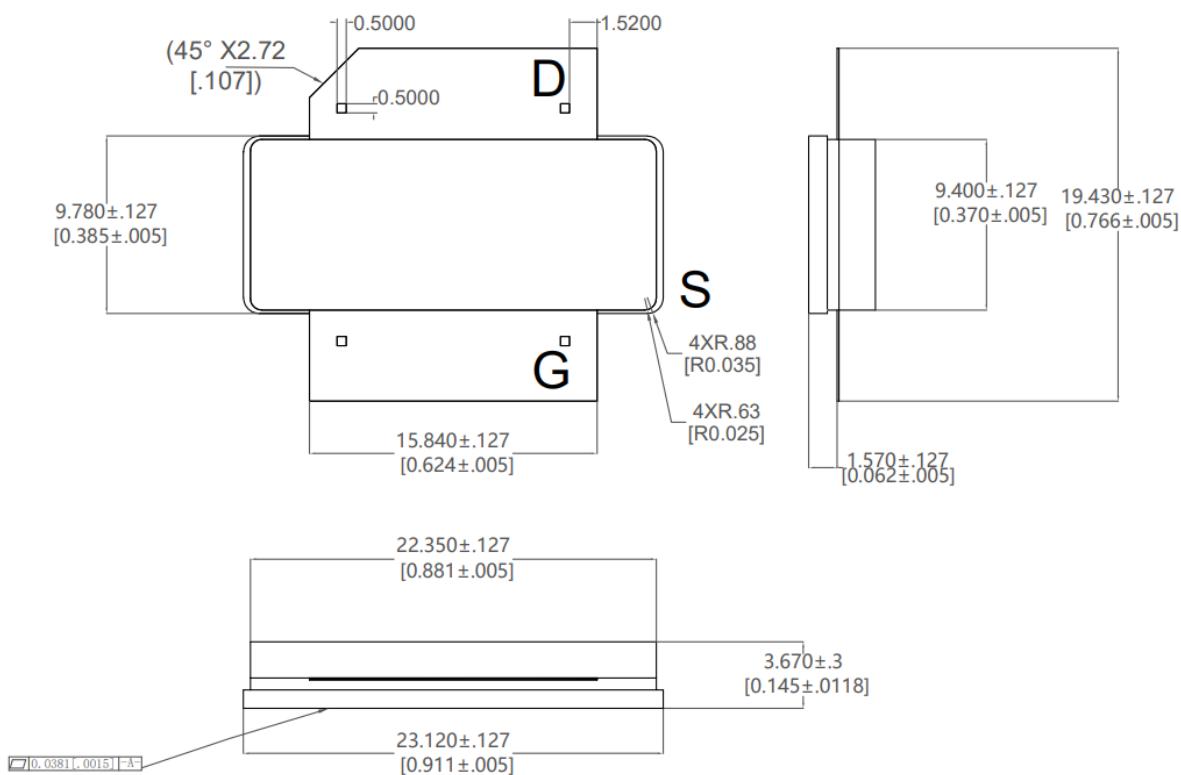
Table 4. Bill of materials of application board (PCB layout upon request)

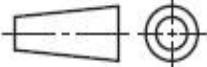
Designator	Comment	Footprint	Quantity
C1	6.8 pF/250V	0805	1
C2	20 pF/250V	0805	1
C3, C4, C5	20 pF/250V	1210	3
C6, C7, C8	10uF/100V	1210	3
C9, C10	470uF/63V		2
R1	10 Ω	0603	1

Package Outline

Flangeless ceramic package;

INP-688-2-EL (C2)



OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-C2					09/27/2018



Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2025/12/31	V1.0	Production Datasheet Creation

Application data based on LSM-25-37

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