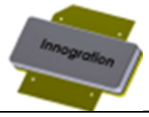
Gallium Nitride 28V,300W,1-2GHz RF Power Transistor

GTAH17300RC2



Description

The GTAH17300RC2 is a 300W，both input and output matched GaN HEMT, ideal for multiple applications from 1-2GHz,.It can support CW, pulse or any modulated signal.

In typical 1.3-1.9G application, it can deliver >300W CW at 28V and >350W at 32V

There is no guarantee of performance when this part is used outside of stated frequencies.

- Typical performance across 1.3-1.9GHz class AB application circuit with device soldered

V_{DS}=28V I_{DQ}=100mA(V_{GS}=-2.75V)

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
1200	54.72	296.7	51.5	14.0	55.47	352.0	53.7
1300	54.57	286.8	52.1	14.5	55.28	337.3	54.1
1400	54.12	258.1	51.2	14.9	55.08	321.8	54.9
1500	53.73	235.9	49.1	15.2	55.09	323.0	55.3
1600	53.71	234.9	46.2	14.0	55.14	326.4	53.7
1700	53.47	222.6	42.8	12.9	55.13	325.9	50.8
1800	53.28	212.9	41.2	13.5	55.31	339.3	50.5
1900	53.31	214.3	43.1	13.8	55.20	330.9	52.1

Applications

- L band power amplifier
- GPS, Beidou jammer
- 1.5GHz LTE amplifier

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

Turning the device ON

1. Set VGS to the pinch--off (VP) voltage, typically –5 V
2. Turn on VDS to nominal supply voltage
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically –5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+150	Vdc
Gate--Source Voltage	V_{GS}	-10 to +2	Vdc
Operating Voltage	V_{DD}	32	Vdc
Maximum gate current	Igs	90	mA
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit

Thermal Resistance, Junction to Case by FEA T_C= 25°C, at Tj=200°C	$R_{\theta JC}$	0.45	°C /W

Table 3. Electrical Characteristics (TA = 25℃ unless otherwise noted)

DC Characteristics (measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	VGS=-8V; IDS=90mA	V_{DSS}		150		V
Gate Threshold Voltage	VDS =10V, ID = 90mA	$V_{GS(th)}$	-4		-2	V
Gate Quiescent Voltage	VDS =50V, IDS=900mA, Measured in Functional Test	$V_{GS(Q)}$		-3.2		V

Ruggedness Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Load mismatch capability	1.2 GHz, Pout=300W Pulsed CW All phase, No device damages	VSWR		10:1		

1.3-1.9G

Figure 3: Network analyzer output, S11 and S21（ VDS=28V VGS=-2.64V IDQ=600mA）

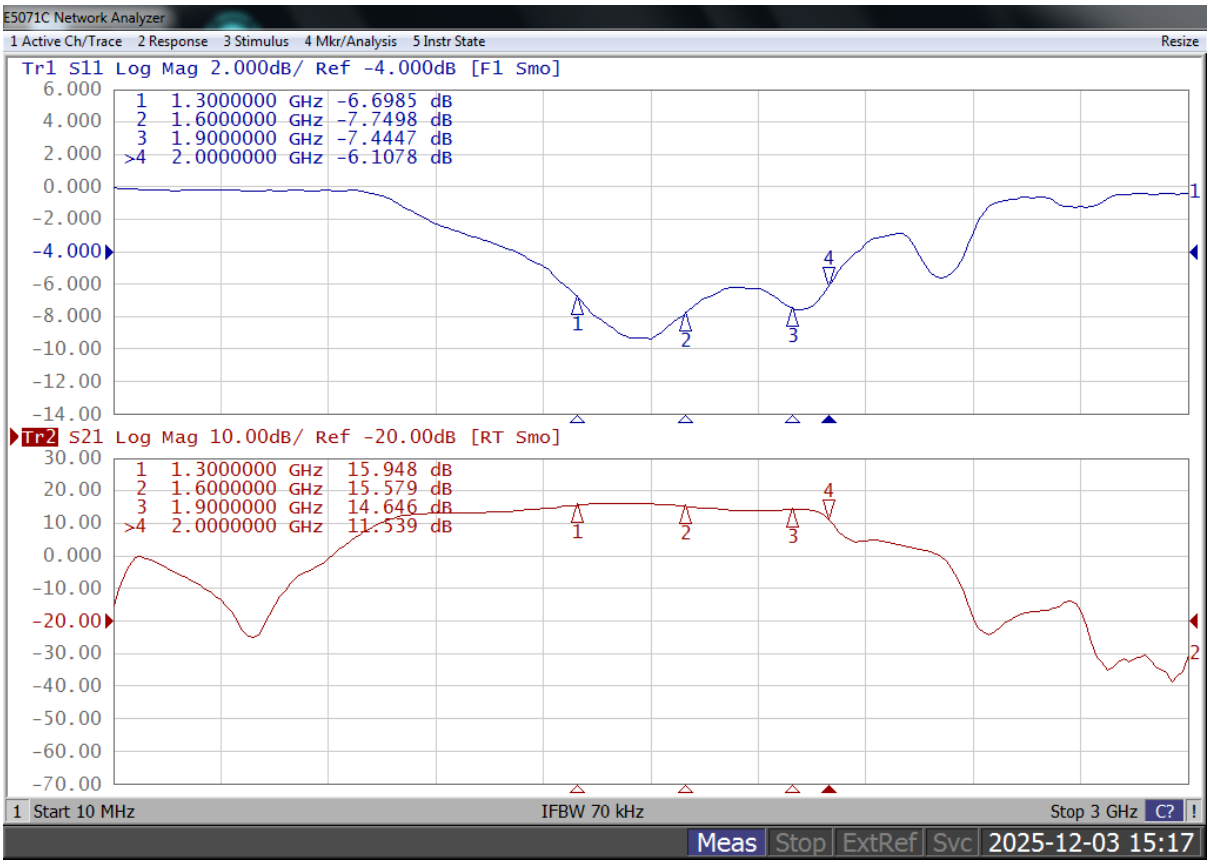


Figure 4: Picture of application board

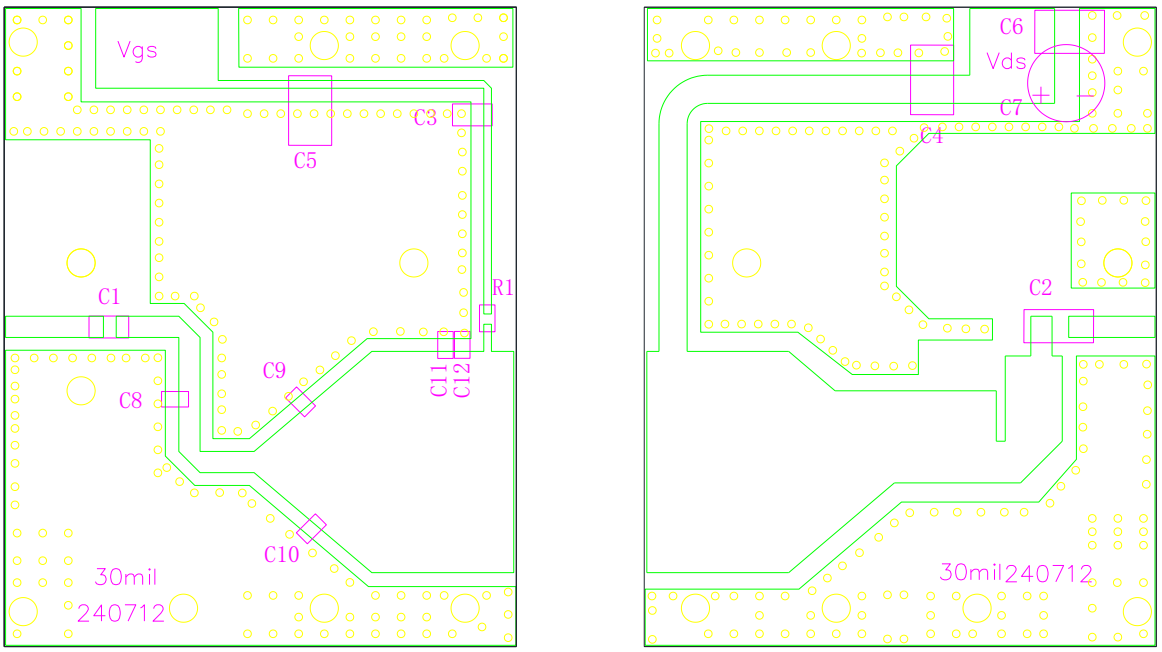


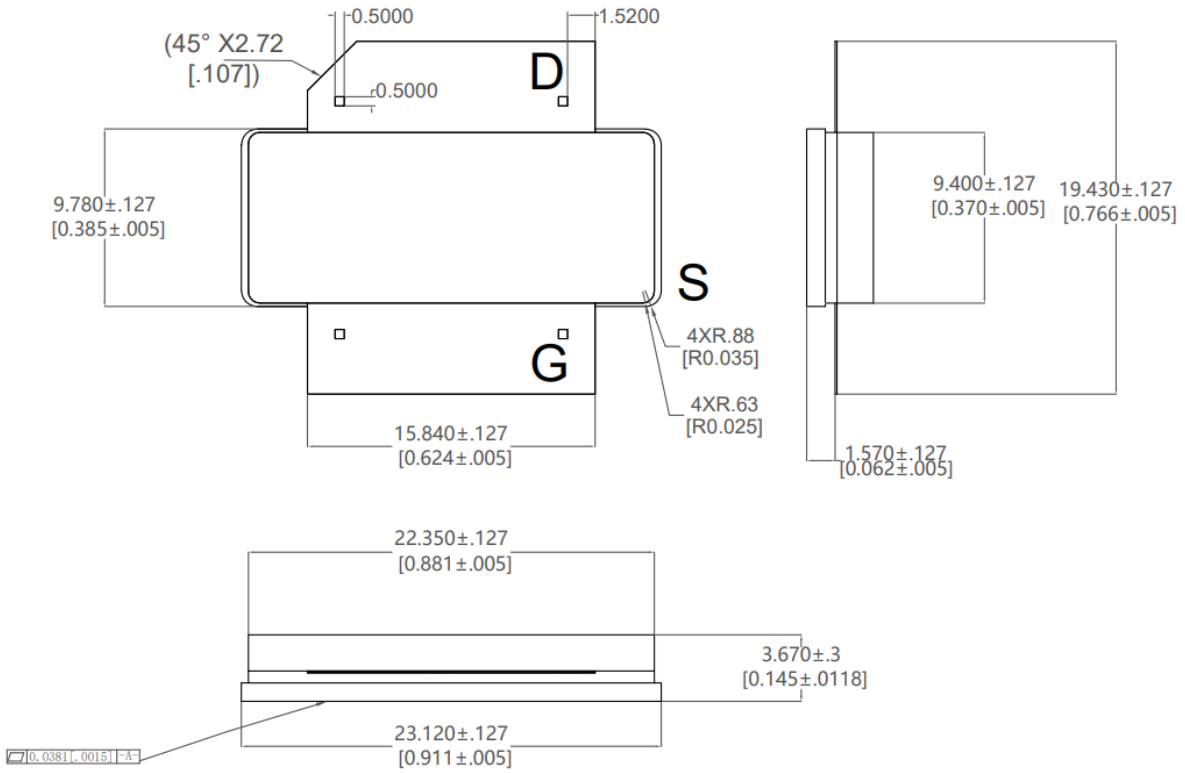
Table 4. Bill of materials of application board (RO4350B 30mil, PCB layout upon request)

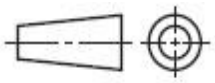
Designator	Comment	Footprint	Quantity
C1	6.8 pF	0603/0805	1
C2, C4,	30 pF	1210	2
C3	30 pF	0603/0805	1
C5, C6	10uF/100V	1210	2
C7	470uF/63V		1
C8	1.5 pF	0603/0805	1
C9, C10	2.7pF	0603/0805	2
C11, C12	2.4 pF	0603/0805	2
R1	10 Ω	0603	1

Package Outline

Flangeless ceramic package;

INP-688-2-EL（C2)



OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-C2					09/27/2018

Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2025/11/4	V1.0	Preliminary Datasheet Creation
2025/12/3	V2.0	Modify with internal matching adjustment for better performance

Application data based on: LSM-25-32

Notice