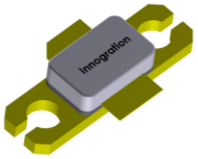
MU1017V LDMOS TRANSISTOR

Document Number: MU1017V
Preliminary Datasheet V1.0

HF-1GHz, 170W, 50V RF LDMOS FETs

MU1017V



Description

The MU1017V is a 170-watt, highly rugged, unmatched LDMOS FET, designed for wide-band commercial and industrial applications at frequencies HF to 1GHz.

•Typical Performance (On Innogration narrow band fixture with device soldered):

Pulsed CW , VDS=50V, VGS=3.3V, Idq=120mA

Freq(MHz)	Pin(dBm)	Pout(W)	Gain(dB)	EFF(%)
700	31.5	180	21	71%

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- 2-30MHz (HF or Short wave communication)
- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 118 -140MHz (Avionics)
- 136-174MHz (Commercial ground communication)
- 160-230MHz (TV VHF III)
- 30-512MHz (Jammer, Ground/Air communication)
- 470-860MHz (TV UHF)
- 100kHz - 1000MHz (ISM, instrumentation)

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	110	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	$R_{\theta JC}$	0.61	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage V_{GS}=0, I_{DS}=1.0mA	$V_{(BR)DSS}$		110		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate--Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600 μA)	V_{GS}(th)	——	2.73	——	V
Gate Quiescent Voltage (V_{DD} = 50 V, I_D = 200 mA, Measured in Functional Test)	$V_{GS(Q)}$	——	3.3	——	V
Common Source Input Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz)	C_{ISS}		130		pF
Common Source Output Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz)	C_{OSS}		50		pF
Common Source Feedback Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz)	C_{RSS}		1.3		pF

Functional Tests (In Demo Test Fixture, 50 ohm system) V_{DD} = 50 Vdc, I_{DQ} = 100mA, f = 700 MHz, Pulsed CW Signal Measurements, Pin=31.5dBm

Power Gain@Pout	G_P	——	21	——	dB
Output Power	Pout	170	180		W
Drain Efficiency@Pout	η_D	——	70	——	%
Input Return Loss	IRL	——	-7	——	dB

TYPICAL CHARACTERISTICS

Figure 1: Pulsed CW Gain and Power Efficiency as a Function of Pout at 700MHz

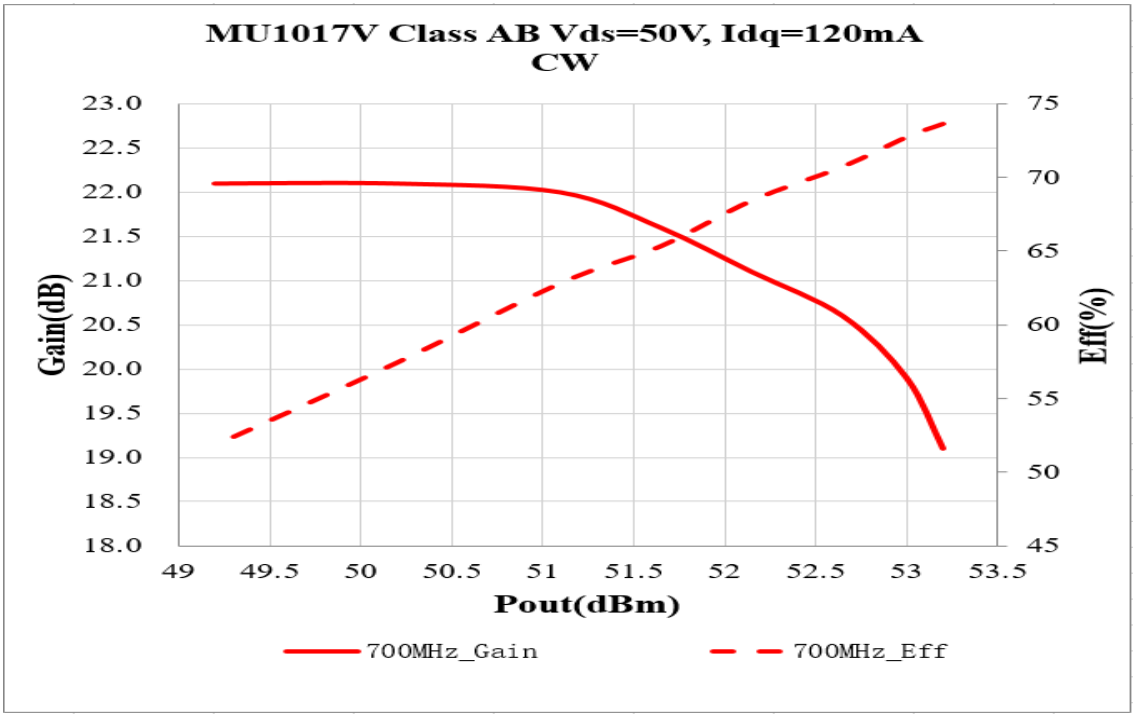
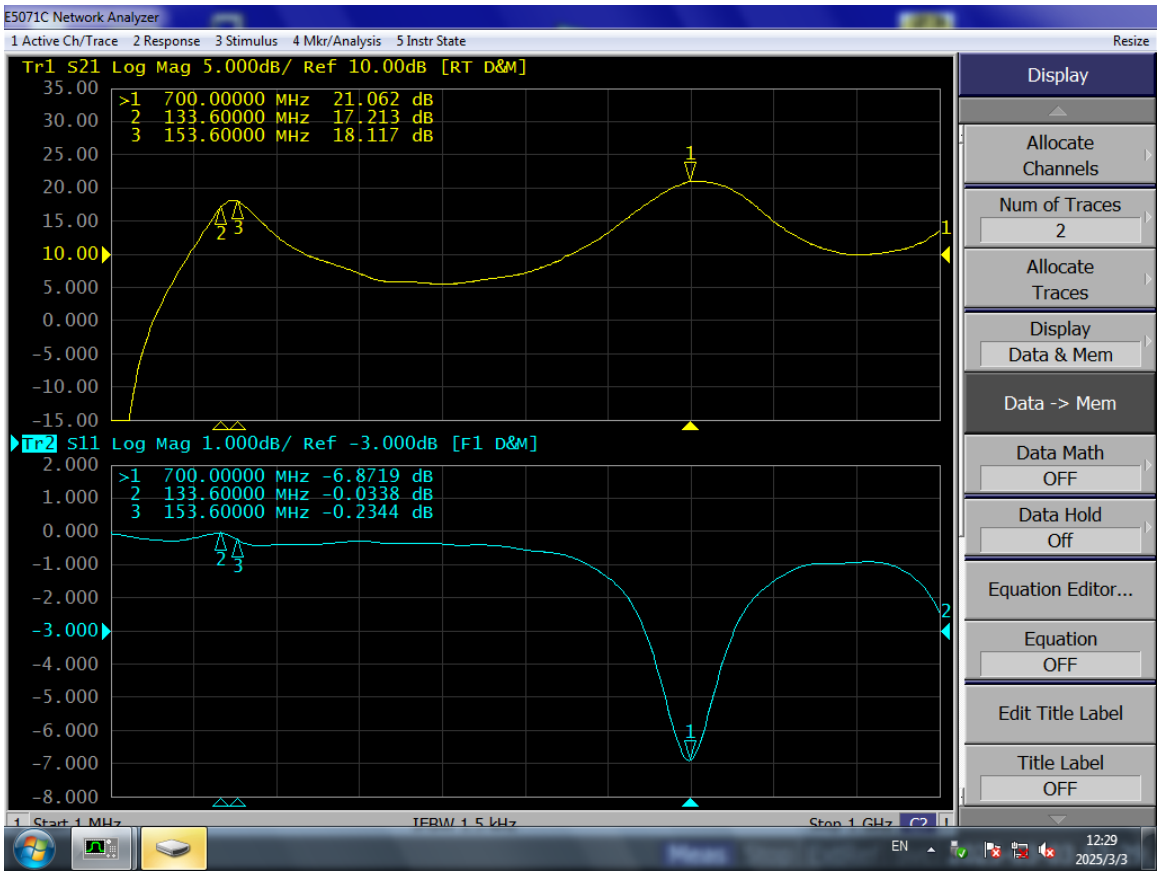
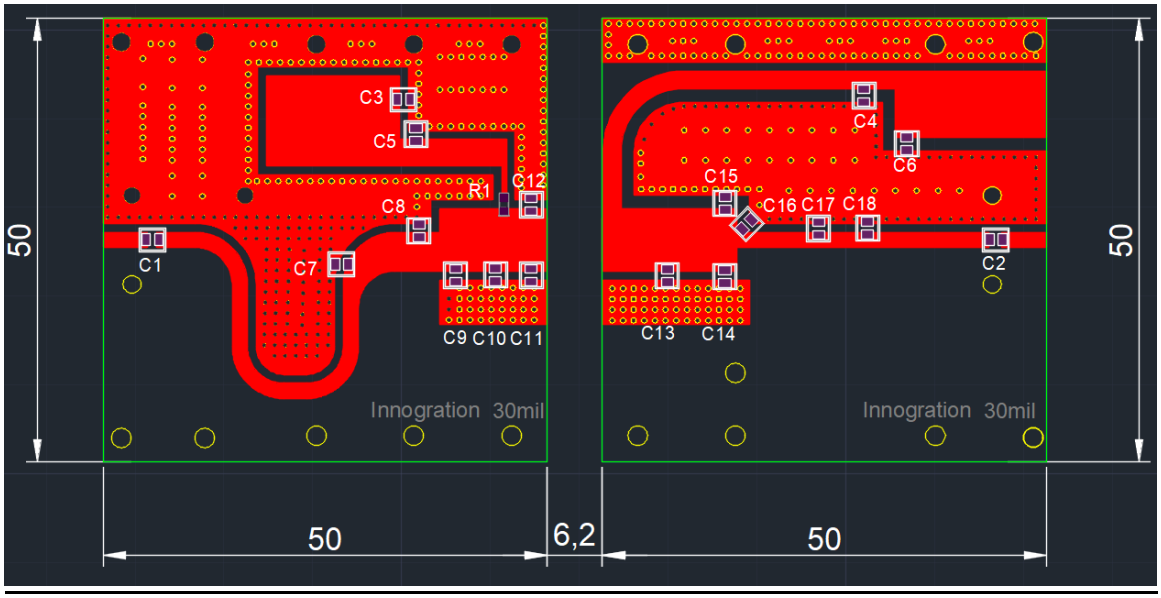


Figure 2: Network analyzer output S11/221



Reference Circuit of Test Fixture Assembly Diagram

700MHz Class AB (Layout file upon request,)

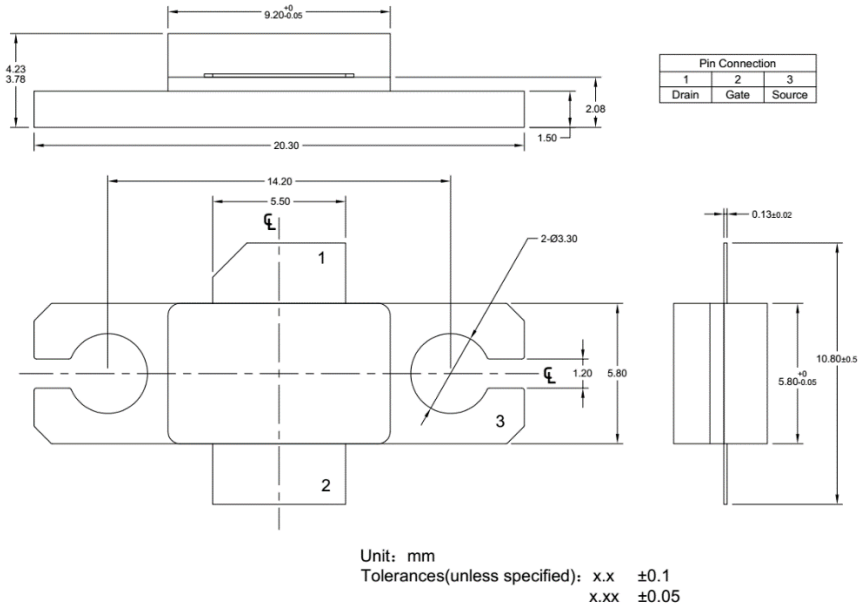


Test Circuit Component Designations and Values

Component	Description	Suggestion
C3,C6	10uF 1210	/
R1	22Ω 0805	/
C1,C2	20pF MQ301111	
C2,C4,C5	100pF MQ301111	
C7,C17	8.2pF MQ301111	
C8,C14,C16	10pF MQ301111	
C9,C10	12pF MQ301111	
C11,C12	18pF MQ301111	
C13	15pF MQ301111	
C15	6.2pF MQ301111	
C18	2.0pF MQ301111	

Package Outline

Flanged ceramic package; 2 leads



OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-GXB					10/10/2017

Figure 1. Package Outline PKG-G2E

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2025/3/5	**V1.0**	**Preliminary Datasheet Creation**

Application data based on SYX-25-09

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