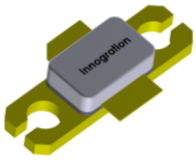
MU0520X LDMOS TRANSISTOR

Document Number: MU0520X
Preliminary Datasheet V1.0

200W, HF-200MHz 28V High Power RF LDMOS

MU0520X



Description

The MU0520X is a 200W single ended 28V LDMOS, highly rugged，unmatched for any applications within HF-200MHz

It supports CW, and pulsed and any modulated signal at either saturated or linear application.

•Typical Performance (On Innogration multiple fixtures with device soldered):

V_{DD} = 28 Volts, I_{DQ} = 150 mA, CW.

Frequency	Pin（dBm）	Gp (dB)	P_{OUT} (W)	η_D (%)	2nd（dB）	3rd （dB）
30MHz	28	25	200	78	-26	-39
40.68MHz	33	20	203	81	-28	-41

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- 2-30MHz (HF or Short wave communication)
- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 118 -140MHz (Avionics)
- 136-174MHz (Commercial ground communication)
- 160-230MHz (TV VHF III)

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+95	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+36	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	$R_{\theta JC}$	0.55	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage V_{GS}=0, I_{DS}=1.0mA	$V_{(BR)DSS}$	95	——		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 75V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate--Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 28V, I_D = 400 μA)	$V_{GS}(th)$	——	2.2	——	V
Gate Quiescent Voltage (V_{DD} = 28 V, I_D = 150 mA, Measured in Functional Test)	$V_{GS(Q)}$	——	3.05	——	V
Common Source Input Capacitance (V_{GS} = 0V, V_{DS} =28 V, f = 1 MHz)	C_{ISS}		187		pF
Common Source Output Capacitance (V_{GS} = 0V, V_{DS} =28 V, f = 1 MHz)	C_{OSS}		79		pF
Common Source Feedback Capacitance (V_{GS} = 0V, V_{DS} =28 V, f = 1 MHz)	C_{RSS}		4.6		pF

Functional Tests (In Demo Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 150mA, f = 150 MHz, Pin=2W, CW Signal Measurements.

Power Gain	G_p	——	20	——	dB
Drain Efficiency@Pout	η_D	——	80	——	%
Output Power	P_{out}	——	200	——	W
Input Return Loss	IRL	——	-7	——	dB

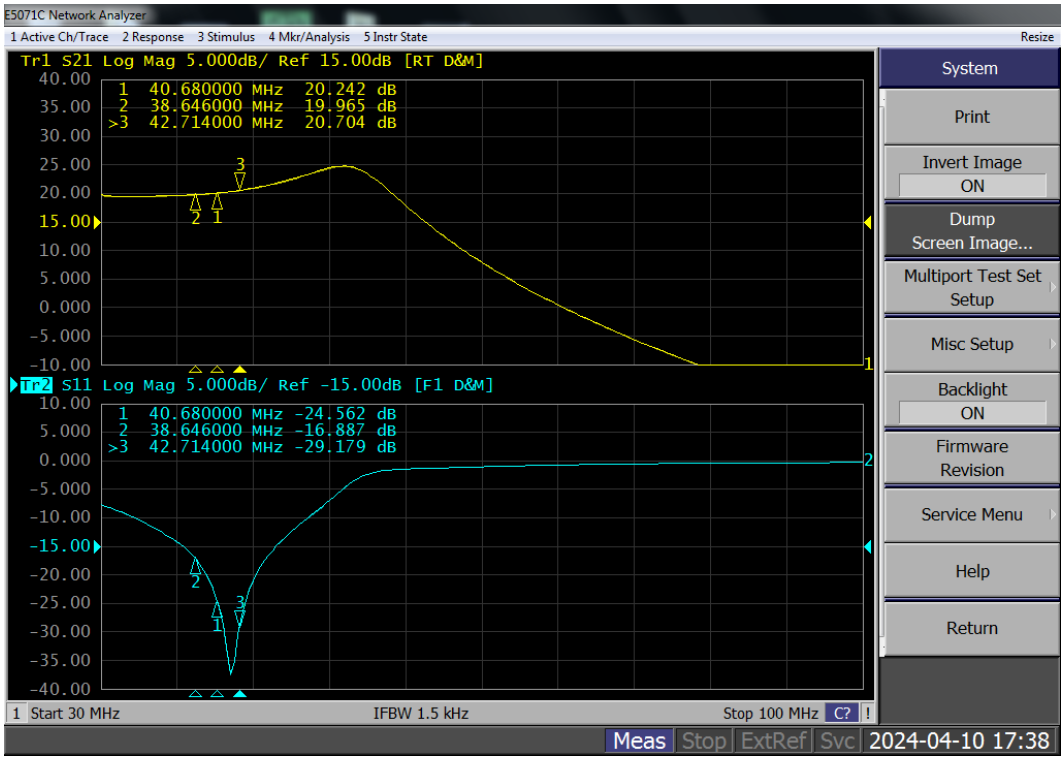
Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 28 Vdc, I_{DQ} = 150 mA, f = 150 MHz

VSWR 20:1 at 200W pulse CW Output Power	No Device Degradation

40.68MHz

TYPICAL CHARACTERISTICS

Figure 1: Network analyzer output S11/221



Reference Circuit of Test Fixture Assembly Diagram (PCB file upon request)

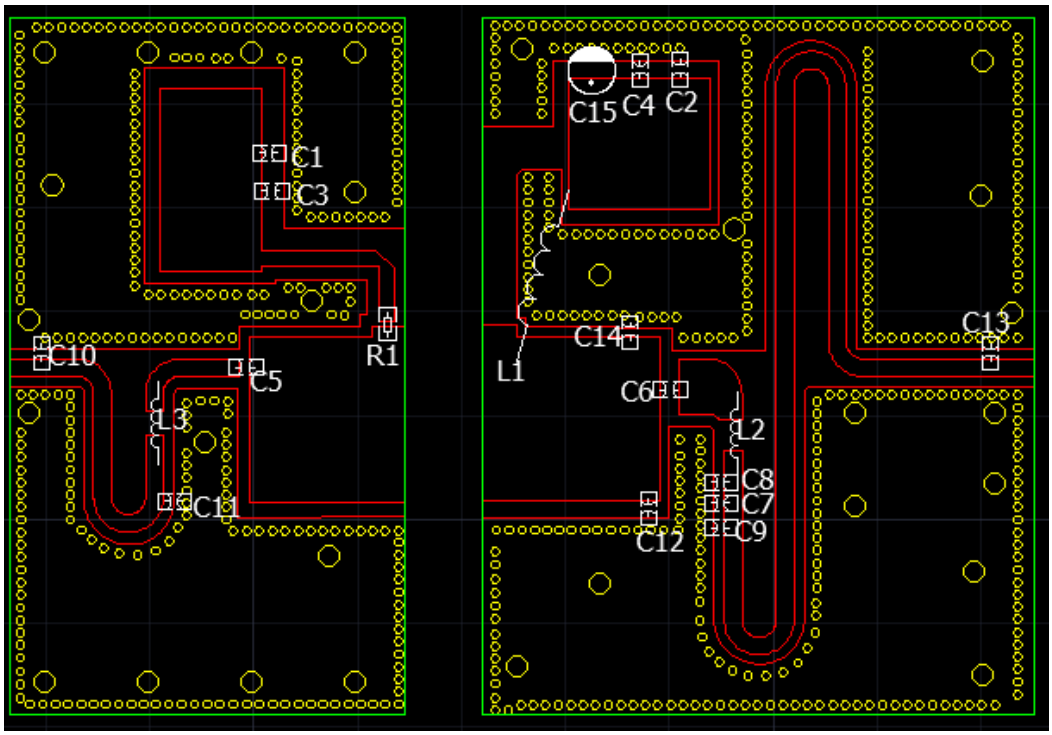
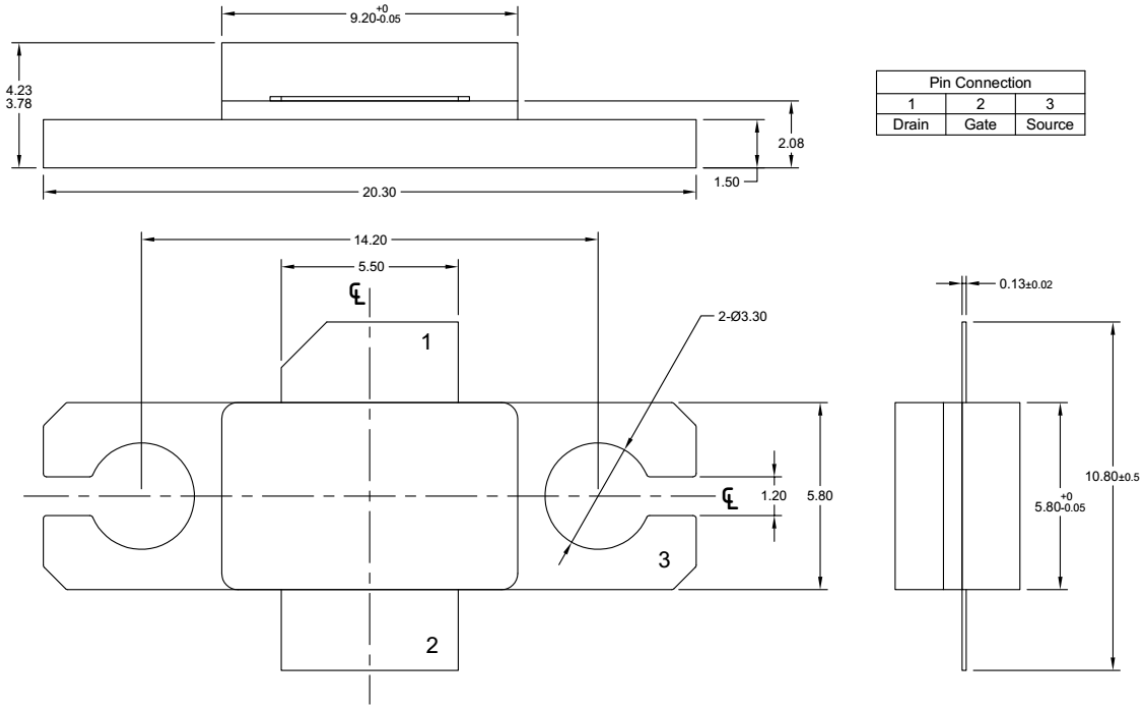


Table 1. Test Circuit Component Designations and Values (40.68MHz)

Component	Description	Suggestion
C1,C2	10uF	10uF/100V
C3~C6	10nF	10nF/100V
C7,C8	150pF	MQ101111
C9	39pF	MQ101111
C10	120pF	MQ101111
C11	47pF	MQ101111
C12	18pF	MQ101111
C13	12pF	MQ101111
C14	200pF	MQ101111
C15	470uF/63V	Electrolytic Capacitor
R1	10Ω	Chip Resistor
L1	1.5mm/5mm，8 turns	
L2	1.5mm/5mm，4 turns	
L3	1.5mm/5mm，6 turns	
PCB	30Mil Rogers4350	

Package Outline

Flanged ceramic package; 2 leads



OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-GXB					10/10/2017

Figure 1. Package Outline PKG-G2E

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2025/4/23	Rev 1.0	Preliminary datasheet

Application data based on TC-24-22/SJJ-25-09

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