ITEV10420B4C LDMOS TRANSISTOR

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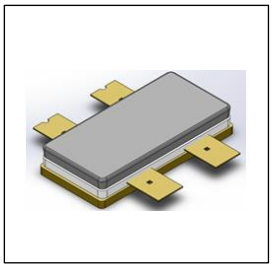
Preliminary Datasheet V1.0

100Wx2, HF to UHF, 28V High Power RF LDMOS FETs



Description

The ITEV10420B4C is a 200-watt, Push Pull, high performance, highly rugged, unmatched LDMOS transistor, designed for any general applications at frequencies from HF to UHF, in new generation highly cost effective open cavity package.

Typical broadband CW performance

Freq (MHz)	Psat (dBm)	Psat (W)	Ids (A)	Pin (dBm)	Gain (dB)	Eff (%)	2nd (dBc)	3rd (dBc)
200	51.63	145.5	7.59	39.47	12.16	68.49	-32	-14.8
300	51.85	153.1	9.67	39.41	12.44	56.55	-31	-8.9
400	51.92	155.6	10.88	39.89	12.03	51.08	-32.3	-24
500	52.46	176.2	13.41	40.16	12.3	46.93	-27.3	-24.3
600	52.65	184.1	14.14	40.99	11.66	46.49	-36.4	-28.7
700	52.76	188.8	13.82	40.31	12.45	48.79	-48.4	-40
800	52.87	193.6	13.16	42.22	10.65	52.55	-46.4	-47.9
900	52.7	186.2	12.82	42.62	10.08	51.87	-41.2	-46.5
1000	51.74	149.3	11.16	42.33	9.41	47.77	-40.5	-41.2

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 136-174MHz (Commercial ground communication)
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- Laser Exciter
- Synchrotron
- MRI
- Plasma generator
- Weather Radar

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+110	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	$R_{\theta JC}$	0.35	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (T_A = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics (per half section)					
Drain-Source Voltage V_{GS}=0, I_{DS}=1.0mA	$V_{(BR)DSS}$		110		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 75V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate--Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 28V, I_D = 600 μA)	$V_{GS}(th)$	——	2.65	——	V
Gate Quiescent Voltage (V_{DD} = 28 V, I_D = 500 mA, Measured in Functional Test)	$V_{GS(Q)}$	——	3.7	——	V

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 28 Vdc, I_{DQ} = 500 mA, f =700MHz, pulse width:100us, duty cycle:10%

Load 10:1 All phase angles, at 200W Pulsed CW Output Power	No Device Degradation

200-1000MHz

Reference Circuit of Test Fixture Assembly Diagram

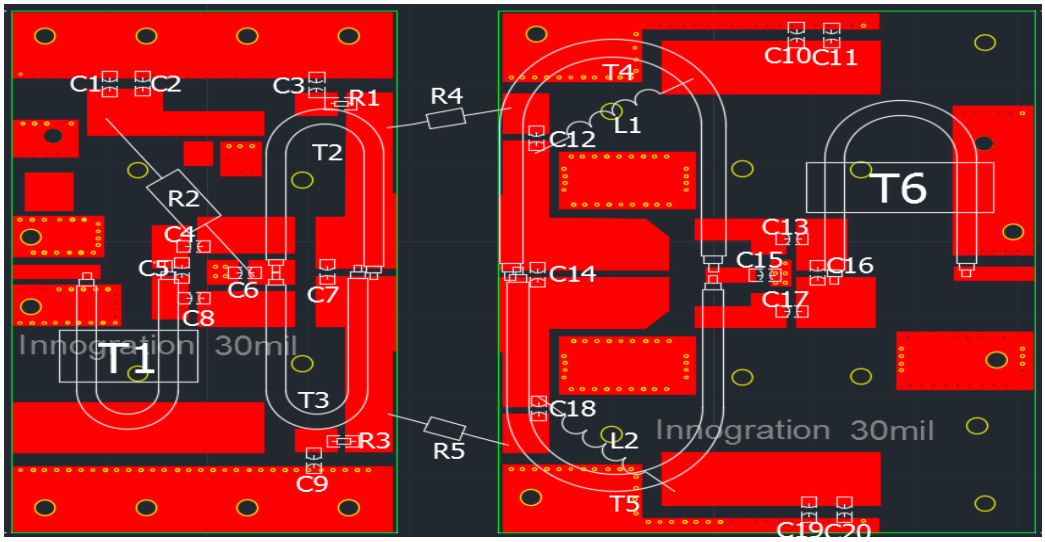
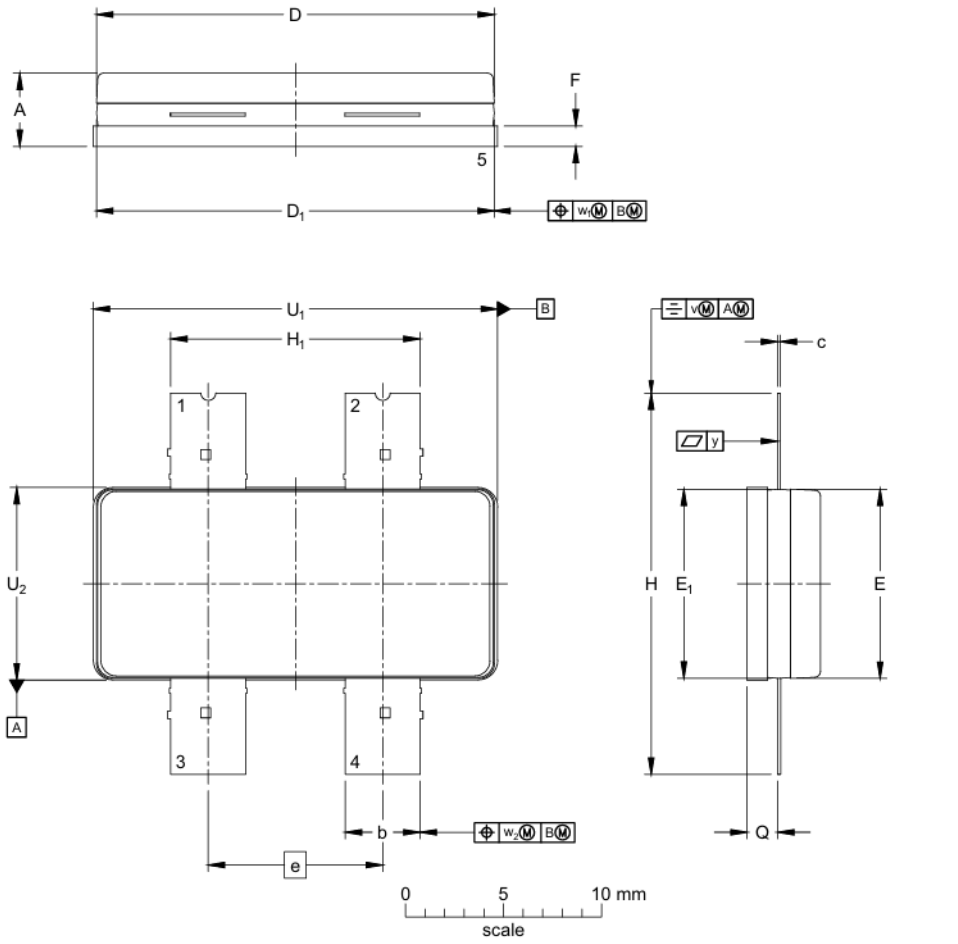


Table 5. Test Circuit Component Designations and Values

C1,C3,C9,C11,C20	10uF/1210	/
C2,C6,C10,C12, C15,C18,C19	560pF/MQ301111	
C4,C8,C13,C17	75pF/MQ301111	
C5	1.8pF//MQ301111	
C7	8.2pF/MQ301111	
C14	5.6pF/MQ301111	
C16	0.8pF/MQ301111	
R1,R3	18Ω/1206	/
R2	300Ω	
R4,R5	330Ω	
L1,L2	1.5mm，2 turns, ϕ=5mm	DIY
T1	50Ω,55mm	RFSFBU-086-50//NXO-20
T2,T3	16.7Ω,40mm	SFF-16.7-1.5
T4,T5	16.7Ω,30mm	SFF-16.7-1.5
T6	50Ω,60mm	RFSFBU-086-50/NXO-20

Earless Flanged Plastic Air Cavity Package; 4 leads



Dimensions

Unit		A	b	c	D	D_1	E	E_1	e	F	H	H_1	$Q^{(1)}$	U_1	U_2	v	w_1	w_2	y
mm	max	4.01	3.91	0.18	20.42	20.37	9.80	9.75		1.14	19.53	12.83	1.68	20.70	9.91	0.50	0.50	0.50	0.10
	nom								8.89										
	min	3.40	3.71	0.13	20.12	20.17	9.50	9.55		0.94	19.33	12.57	1.45	20.50	9.70				

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2025/4/24	Rev 1.0	Preliminary Datasheet Creation

Application data based on SJJ-25-08

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