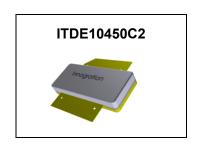
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915MHz, 450W, 40V High Power RF LDMOS FETs

Description

The ITDE10450C2 is a 450-watt, internally matched LDMOS FET, designed for ISM applications including RF Energy at 915MHz. It Can be used in Class AB/B and Class C configuration, supporting both CW and pulsed signal

In typical application using 2*ITDE10450C2 in parallel, it can deliver more than 900W CW with high efficiency, see its standalone application report



•Typical Performance using single **ITDE10450C2** (On Innogration fixture with device soldered): VDD = 40 Volts, I_{DQ} = 50 mA, CW signal

Freq(MHz)	Pin(dBm)	Pout(dBm)	Pout(W)	IDS(A)	Gain(dB)	EFF(%)
915	40	56.7	470	16.7	16.7	70.0%

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Excellent thermal stability, low HCI drift

- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- · Pb-free, RoHS-compliant

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
DrainSource Voltage	V _{DSS}	95	Vdc
GateSource Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+42	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	Tc	+150	°C
Operating Junction Temperature	TJ	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case	Do 10	0.3	0C/M
T _C = 85°C, T _J =200°C, DC test	R⊕JC	0.3	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class		
Human Body Model (per JESD22A114)	Class 2		

Table 4. Electrical Characteristics (TA = 25 C unless otherwise noted)

Characteristic	Symbol	Min	Тур	Max	Unit
DC Characteristics (per half section)					
Drain-Source Breakdown Voltage	$V_{\scriptscriptstyle DSS}$	95			V
(V _{GS} =0V; I _D =100uA)	V DSS	95			V
Zero Gate Voltage Drain Leakage Current				10	^
$(V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V})$	I _{DSS}			10	μΑ



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GateSource Leakage Current					
$(V_{GS} = 6 \text{ V}, V_{DS} = 0 \text{ V})$	Igss			1	μΑ
Gate Threshold Voltage	V (III)		2.0		V
$(V_{DS} = 40V, I_{D} = 600 \text{ uA})$	$V_{\sf GS}(th)$		2.0		V
Gate Quiescent Voltage		2.4	2.02	2.4	V
(V _{DD} = 40 V, I _{DQ} = 100 mA, Measured in Functional Test)	$V_{GS(Q)}$	2.1	2.62	3.1	V

Functional Tests (On Innogration Test Fixture, 50 ohm system) : V_{DD} =40 Vdc, I_{DQ} = 50 mA, f = 915 MHz, Pin=40dBm CW Signal Measurements.

Power Gain	Gp	 16.5	 dB
Drain Efficiency @ P _{OUT}	η _D	 70	%
Output Power	P _{out}	 450	 W
Input Return Loss	IRL	 -7	 dB

Load Mismatch (In Innogration Test Fixture, 50 ohm system): $V_{DD} = 40 \text{ Vdc}$, $I_{DQ} = 50 \text{ mA}$, f = 915 MHz

VSWR 10:1 at 450W Output Power	No Device Degradation
at all Phase Angles, pulsed CW, 100us, 10%	



Reference Circuit of Test Fixture Assembly Diagram 1*ITDE10450C2

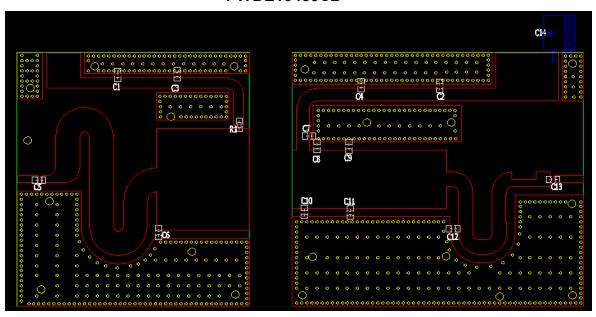


Figure 1. Test Circuit Component Layout

Table 1. Test Circuit Component Designations and Values

Component	Description	Suggestion
C1,C2	10Uf	10Uf/100V
C3,C4,C5	56Pf	MQ101111
C6	7.5Pf	MQ101111
C14	2000Uf/63V	Electrolyic Capacitor
R1	10 Ω Chip Resistor	
C7	9.1Pf	MQ101111
C8	12Pf MQ101111	
C9	8.2Pf	MQ101111
C10	11Pf	MQ101111
C11	10Pf	MQ101111
C12	0.5Pf MQ101111	
C13	47Pf MCM-1-300V-D-470J	
PCB	30mil Rogers 4350B	



TYPICAL CHARACTERISTICS

Figure 2. Drain Efficiency and Power Gain as Function of CW Output Power

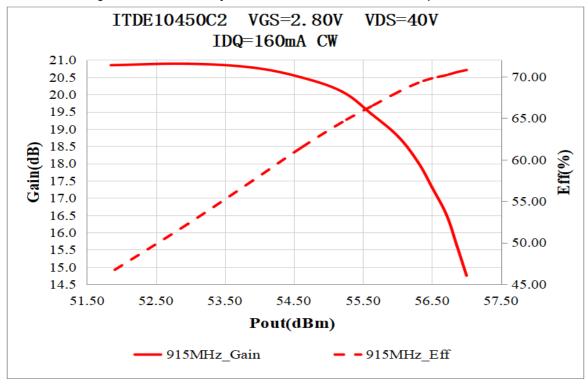
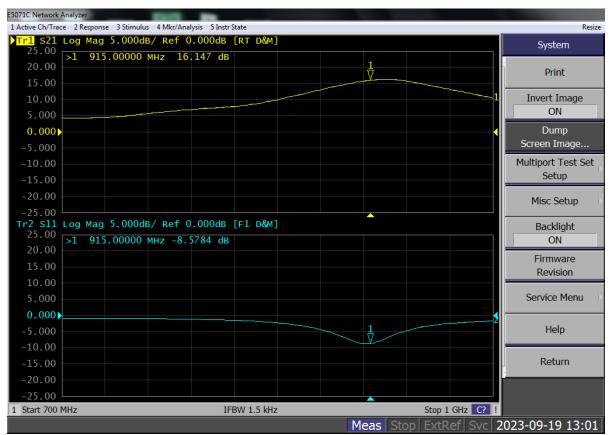
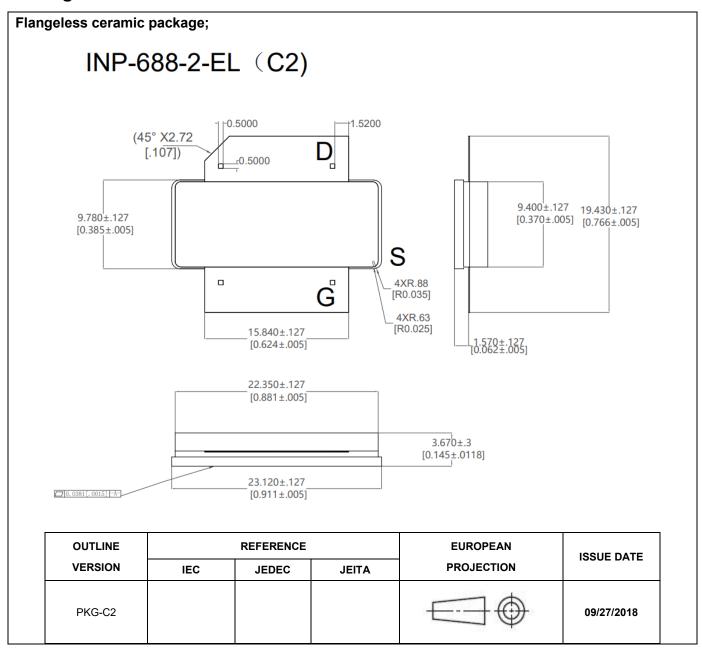


Figure 3. Network analyzer output S11/S21





Package Outline



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Revision history

Table 6. Document revision history

Date	Revision	Datasheet Status
2022/1/12	Rev 1.0	Preliminary Datasheet
2023/9/19	Rev 1.1	Add single device application data
2023/10/20	Rev 1.2	Modify the error of thermal resistor and product rating on page 1 and 2
2025/2/16	Rev 1.3	Update according to improvement of 2 pcs combination
2025/4/24	Rev 1.4	Delete 2 pcs combination result and present by another newer test report

Application data based on JF-21-14/TC-23-60, LSM-25-02

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