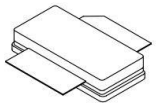
MK2210S LDMOS TRANSISTOR

Document Number: MK2210S
Preliminary Datasheet V1.0

1.7-2.2Hz, 100W, 28V High Power RF LDMOS FETs

MK2210S



Description

The MK2210S is a 100-watt, internally matched LDMOS FETs, designed for wideband applications from 1700 to 2200MHz.

It can be used in Class AB/B and Class C for all pulsed and CW formats.

- Typical Performance (on wideband board with device soldered):

Vds=28V Idq=800mA CW

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
1700	50.96	124.8	55.5	14.75	51.92	155.5	58.4
1800	50.76	119.2	53.1	15.01	51.74	149.4	55.8
1900	50.15	103.6	48.5	14.9	51.54	142.6	53.8
2000	50.47	111.5	52.2	14.82	51.71	148.1	57.2
2100	50.13	103.2	53.2	14.69	51.28	134.2	57.2
2200	49.54	90.0	52.1	14.29	50.66	116.5	55.8

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	65	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+32	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case Case Temperature 80°C, DC Test	$R_{\theta JC}$	0.55	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Zero Gate Voltage Drain Leakage Current (VDS = 65V, VGS = 0 V)	I_{DSS}			100	μA

Zero Gate Voltage Drain Leakage Current (VDS = 28 V, VGS = 0 V)	I_{DSS}			1	μA
Gate--Source Leakage Current (VGS = 6 V, VDS = 0 V)	I_{GSS}			1	μA
Gate Threshold Voltage (VDS =28V, ID = 300 μA)	$V_{GS}(th)$		2		V
Gate Quiescent Voltage (VDD = 28 V, ID = 1000 mA, Measured in Functional Test)	$V_{GS(Q)}$		3.2		V

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 28Vdc, I_{DQ} = 100 mA, f = 2200 MHz

VSWR 5:1 at 100W Pulsed CW Output Power	No Device Degradation

TYPICAL CHARACTERISTICS

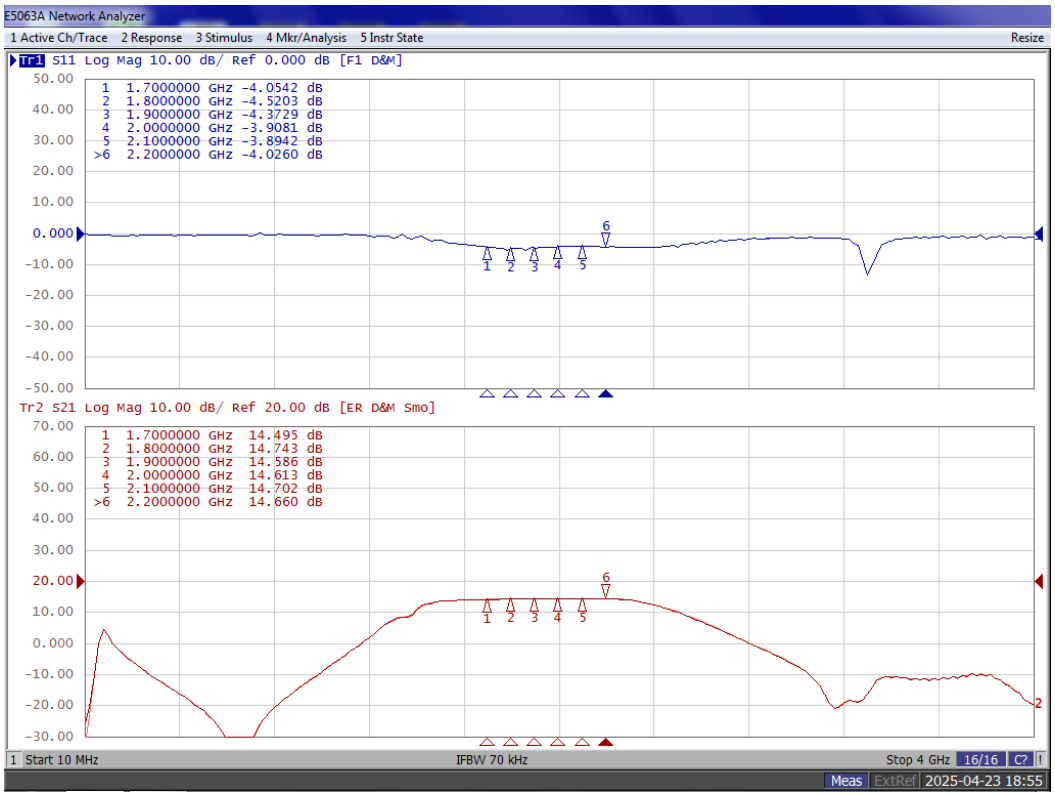


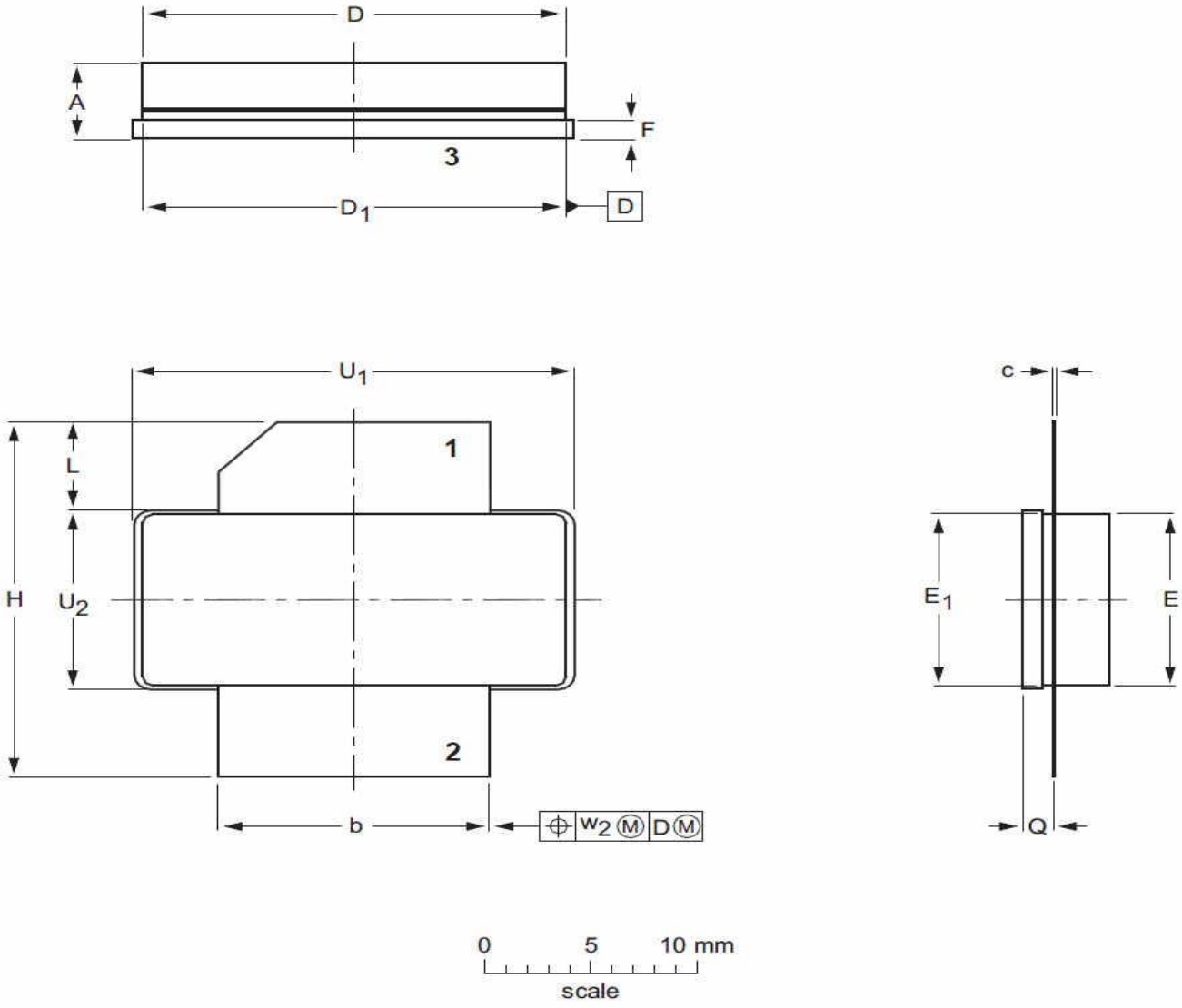
Figure 1. Network analyzer output S11/S21, Idq=800mA, Vds=28V

Reference Circuit of Test Fixture Assembly Diagram
(Layout file upon request)

Component	Value	Quantity
U1	MK2210S	1
C1、C4、C5、C6	36pF	4
C2	1.2pF	1
C3	0.8pF	1
C7、C8、C9、C10	10uF/63V	4
R1	10Ω	1
C11	470uF/63V	1

Package Outline

Earless flanged ceramic package; 2 leads



UNIT	A	b	c	D	D_1	E	E_1	F	H	L	Q	U_1	U_2	W_2
mm	4.72	12.83	0.15	20.02	19.96	9.50	9.53	1.14	19.94	5.33	1.70	20.70	9.91	0.25
	3.43	12.57	0.08	19.61	19.66	9.30	9.25	0.89	18.92	4.32	1.45	20.45	9.65	
inches	0.186	0.505	0.006	0.788	0.786	0.374	0.375	0.045	0.785	0.210	0.067	0.815	0.390	0.010
	0.135	0.495	0.003	0.772	0.774	0.366	0.364	0.035	0.745	0.170	0.057	0.805	0.380	

OUTLINE VERSION	REFERENCE				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
PKG-B2						03/12/2013

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2025/4/25	Rev 1.0	Preliminary Datasheet Creation

Application data based on ZYX-25-10

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