RF LDMOS 12.5V 30W Transistor, L band

ITCN15030A2C

Description

The ITCN15030A2C is a 30W RF LDMOS, designed for multiple applications, within L band. The transistor is available in new generation highly cost effective open cavity package. It can be used in CW, Pulse and multiple modulation mode.

•Typical RF Performance On Innogration fixture

V_{DD} =12.5 V, I_{DQ} =200 mA, CW

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
1400	45.13	32.6	55.4	15.42	45.97	39.6	59.3
1450	44.48	28.1	55.6	16.15	45.42	34.8	59.9
1500	44.01	25.2	55.3	14.93	44.95	31.3	59.5

V_{DD} =12.5 V, I_{DQ} =810 mA, WCDMA 1 Carrier

Freq (MHz)	Pout (dBm)	ACPR (dBc)	Gain (dB)	Eff (%)
1400	32	-47	17.9	10.9
1450	32	-46	18.9	11.3
1500	32	-46.5	17.7	11.5

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- L band amplifier
- GPS

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+40	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+13.6	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	$R_{\theta JC}$	0.6	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

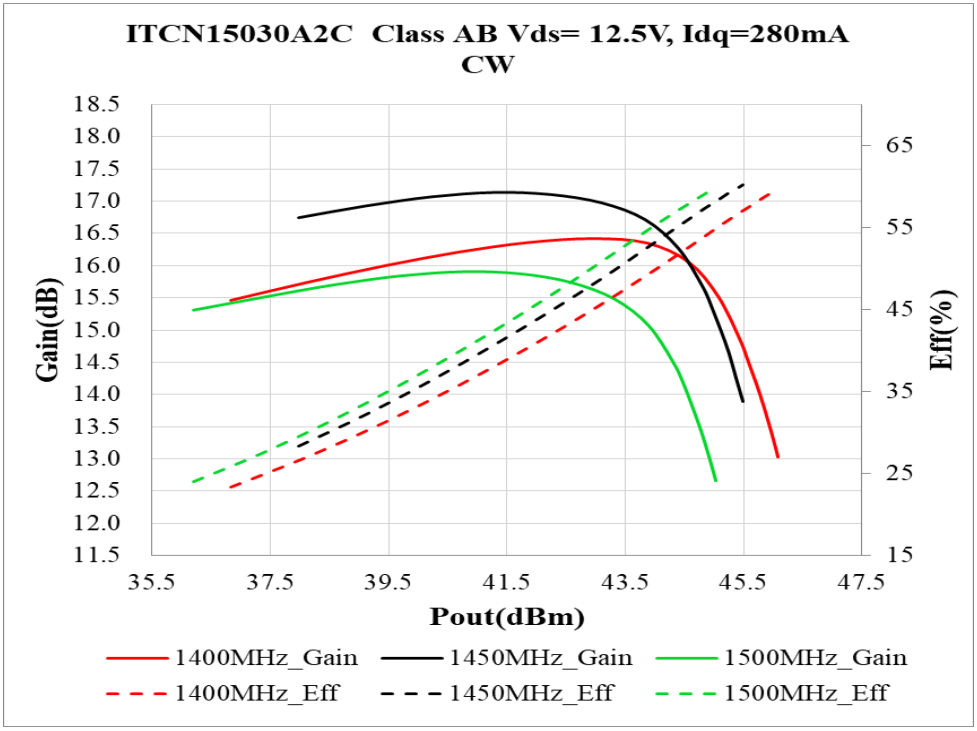
Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage V_{GS}=0, I_{DS}=100uA	$V_{(BR)DSS}$		43		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 12.5V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate--Source Leakage Current (V_{GS} = 9 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 12.5V, I_D = 600 μA)	$V_{GS(th)}$	2		——	V
Gate Quiescent Voltage (V_{DD} = 12.5V, I_D = 800mA, Measured in Functional Test)	$V_{GS(Q)}$	——	2.9	——	V

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 12.5Vdc, I_{DQ} = 800 mA, f = 1500 MHz

VSWR 10:1 at 30W pulse CW Output Power	No Device Degradation

TYPICAL CHARACTERISTICS

1.4-1.5GHz application



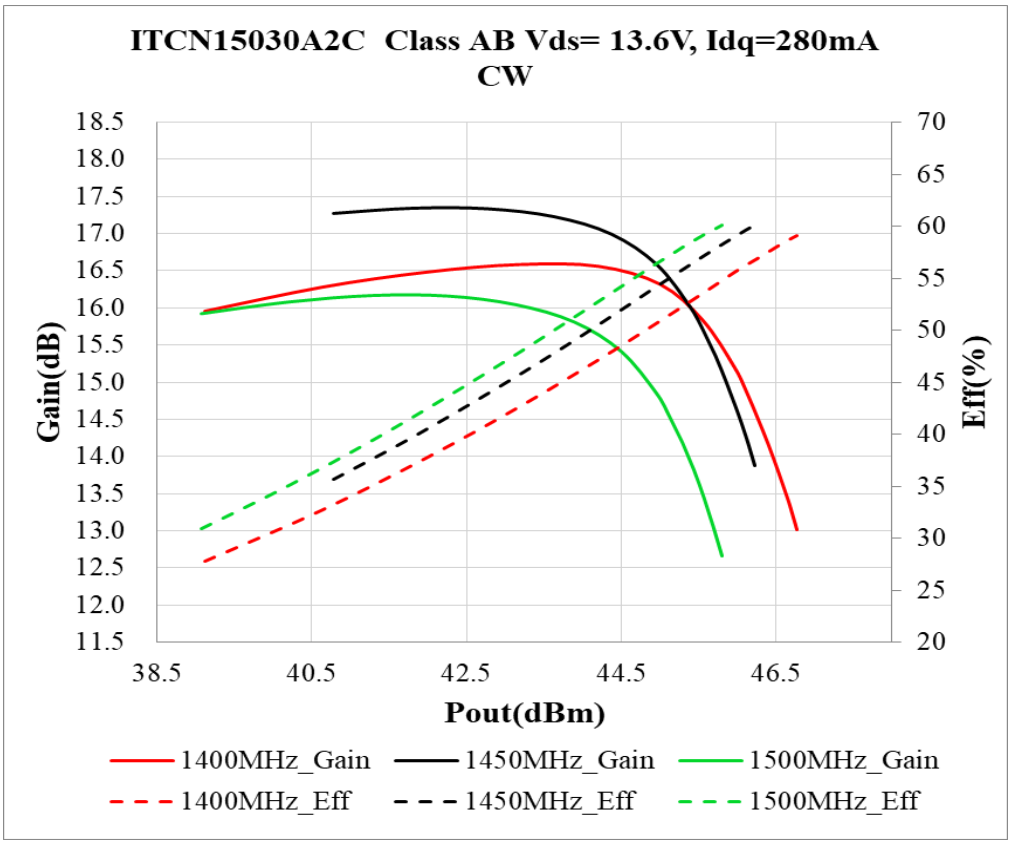


Figure 2. Power Gain and Drain Efficiency as Function of Pulse Output Power at 12.5V/13.6V power supply

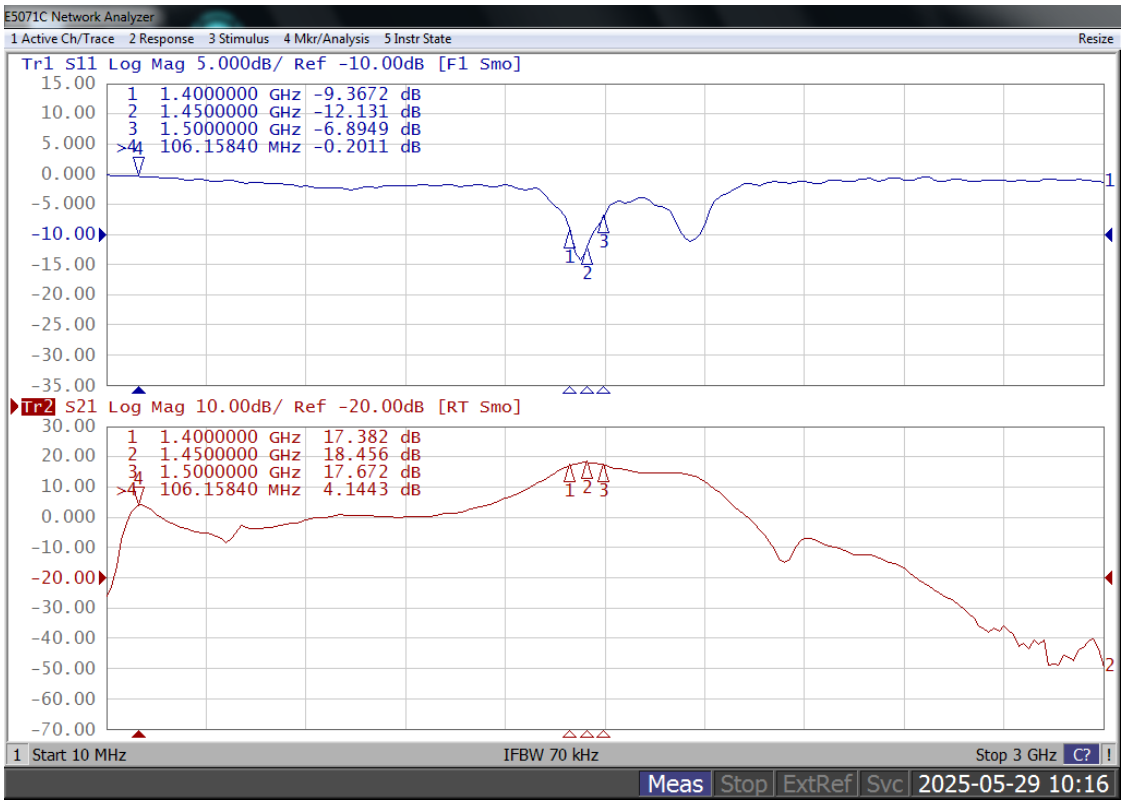
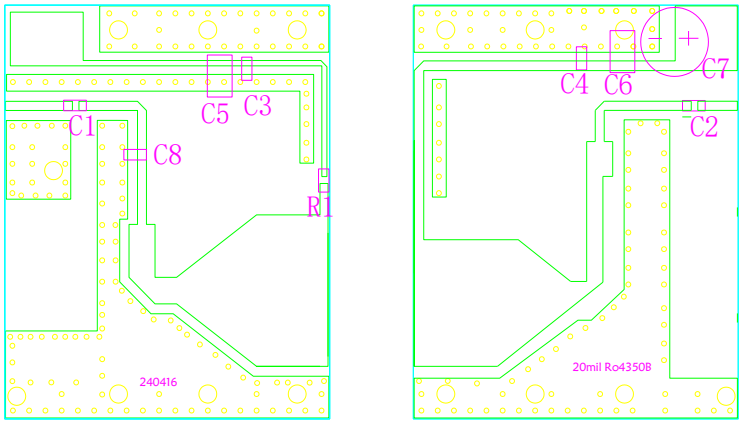


Figure 3. Network analyzer output S11/S21 VDS = 12.5Vdc, Idq= 800mA

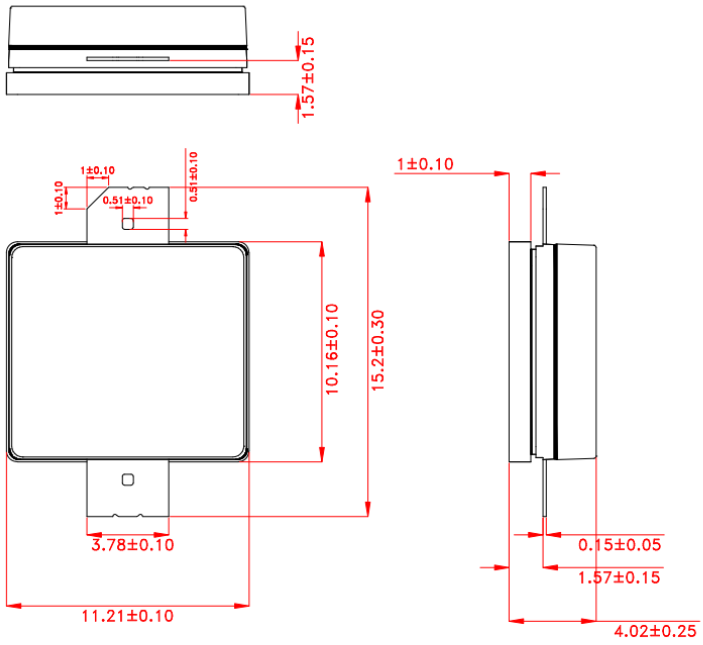
Reference Circuit of Test Fixture Assembly Diagram

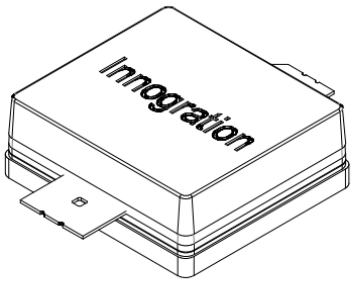
RO4350B 20mils(Layout upon request)



Designator	Comment	Footprint	Quantity
C1,	4.7pF	0603/0805	1
C2, C3, C4,	47pF	0603/0805	3
C5, C6	10 uF/100V	1210	2
C7	470 uF/63V		1
C8	2.7pF	0603/0805	1
R1	10 Ω	0603	1

Package Dimensions





Unit:mm

Tolerance ±0.10mm,Except as Noted.

Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2025/5/29	V1.0	Datasheet Creation

Application data based on LSM-25-14

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