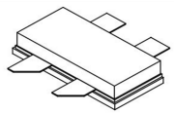
GaN ,0.4-3GHz full band 100W transistor

GTAH30140BY



Description

The GTAH30140BY4 is a 28V 140W capable, both input and output matched GaN HEMT, ideal for multiple applications below 3GHz. **In typical wideband 0.4-3GHz application, it can deliver >100W across the full band**

- Typical performance across 0.4-3GHz class AB application circuit with device soldered

CW signal,Idq=250mA

Freq (MHz)	Psat (dBm)	Psat (W)	IDS (A)	Pin (dBm)	Gain (dB)	Eff (%)	2nd （dBc）	3rd （dBc）
400	50.30	107.2	7.30	41.10	9.20	52.42	-10.20	-10.90
500	51.65	146.2	7.90	36.90	14.75	66.10	-19.40	-12.90
600	51.40	138.0	6.68	41.44	9.96	73.80	-28.30	-12.80
700	50.14	103.3	5.23	41.99	8.15	70.52	-21.60	-11.70
800	50.57	114.0	5.87	41.07	9.50	69.38	-17.30	-10.50
900	50.63	115.6	6.34	39.97	10.66	65.13	-14.80	-12.20
1000	50.56	113.8	6.60	39.45	11.11	61.56	-15.70	-15.70
1100	50.64	115.9	6.51	42.05	8.59	63.57	-14.40	-14.50
1200	50.52	112.7	6.57	39.84	10.68	61.27	-12.50	-13.20
1300	50.05	101.2	6.56	41.08	8.97	55.07	-10.60	-15.40
1400	50.26	106.2	8.21	41.73	8.53	46.18	-12.90	-19.50
1500	50.90	123.0	9.11	41.32	9.58	48.23	-12.30	-26.80
1600	51.42	138.7	10.04	40.20	11.22	49.33	-12.80	-25.10
1700	51.17	130.9	9.70	40.26	10.91	48.20	-13.60	-27.70
1800	50.98	125.3	9.56	41.51	9.47	46.81	-13.60	-29.30
1900	50.97	125.0	8.97	41.16	9.81	49.78	-15.60	-29.00
2000	50.01	100.2	8.02	40.88	9.13	44.63	-18.20	-27.30
2100	50.14	103.3	7.66	41.35	8.79	48.15	-17.60	-27.70
2200	50.89	122.7	8.48	42.20	8.69	51.69	-25.10	-35.00
2300	50.23	105.4	7.54	41.15	9.08	49.94	-29.40	-38.30
2400	50.89	122.7	9.47	42.08	8.81	46.29	-26.20	-47.30
2500	50.53	113.0	9.61	41.61	8.92	41.99	-39.70	-40.30
2600	50.17	104.0	9.51	40.61	9.56	39.05	-44.30	-38.60
2700	51.52	141.9	13.30	41.70	9.82	38.11	-42.30	-36.00
2800	52.08	161.4	14.15	42.70	9.38	40.75	-51.40	-49.60
2900	51.91	155.2	12.90	43.08	8.83	42.98	-39.70	-44.00
3000	51.67	146.9	11.34	42.90	8.77	46.26	-33.30	-44.00

Applications

- S/L/P band power amplifier

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

Turning the device ON

1. Set VGS to the pinch--off (VP) voltage, typically –5 V
2. Turn on VDS to nominal supply voltage
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically –5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

Figure 1: Pin Connection definition

Transparent top view (Backside grounding for source)

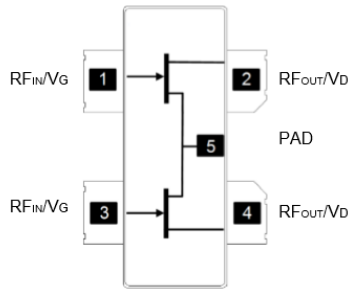


Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+150	Vdc
Gate--Source Voltage	V_{GS}	-10 to +2	Vdc
Operating Voltage	V_{DD}	36	Vdc
Maximum gate current	Igs	36	mA
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case by FEA T_C= 85°C, at Pout=100W CW at 3GHz	$R_{\theta JC}$	1	°C /W

Table 3. Electrical Characteristics (TA = 25℃ unless otherwise noted)

DC Characteristics (measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	VGS=-8V; IDS=36mA	V_{DSS}		150		V
Gate Threshold Voltage	VDS =10V, ID = 36mA	$V_{GS(th)}$	-4		-2	V
Gate Quiescent Voltage	VDS =28V, IDS=110mA, Measured in Functional Test	$V_{GS(Q)}$		-2.57		V

Ruggedness Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Load mismatch capability	GHz, Pout=100W Pulsed CW All phase, No device damages	VSWR		10:1		

Figure 2: Median Lifetime vs. Channel Temperature

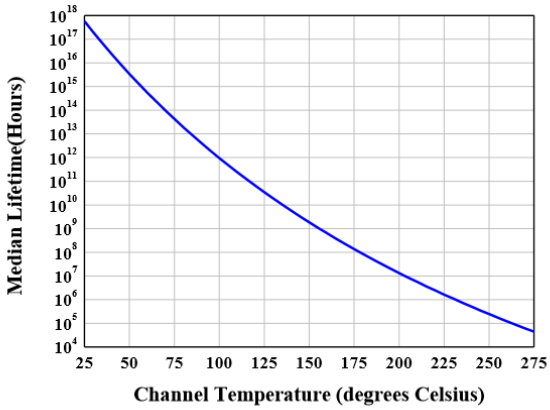


Figure 3: Picture of application board 0.4-3GHz class AB

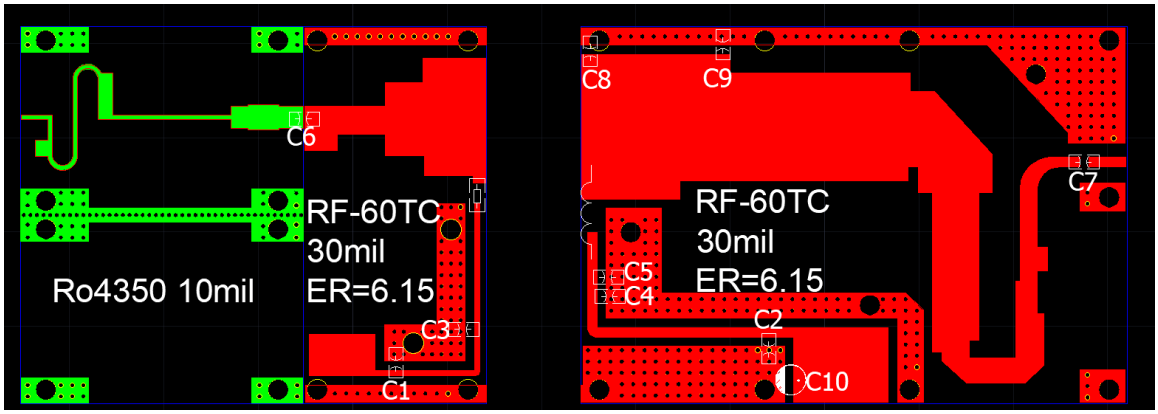
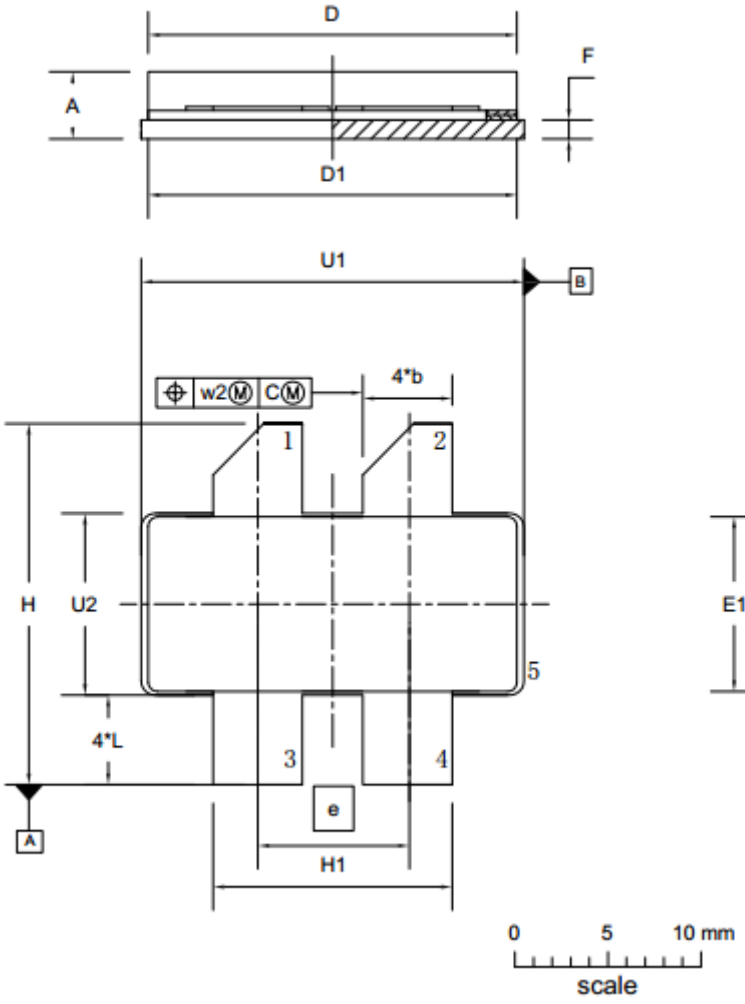


Table 4. Bill of materials of application board (PCB layout upon request)

Component	Description	Suggestion
C1~C2	10uF/200V-1812	Ceramic multilayer capacitor
C3	39pF	
C4	100pF	
C5	200pF	
C6,C7	36pF	
C8,C9	0.5pF	
C10	470uF/63V	Electrolytic Capacitor
R1	51Ω*3-1206	Chip Resistor
L1	1mm wire，3mm innerdiameter，3turns	DIY
PCB	Red：RF-60TC,30mil，er=6.15 green： Rogers4350,10mil	

Earless Flanged Ceramic Package; 4 leads



Drain		Gate		Source
1	2	3	4	5

UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H1	L	Q	U_1	U_2	W_1	W_2
mm	4.72 3.43	4.67 4.93	0.15 0.08	20.02 19.61	19.96 19.66	7.90	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	12.98 12.73	5.33 4.32	1.70 1.45	20.70 20.45	9.91 9.65	0.25	0.51
inches	0.186 0.135	0.194 0.184	0.006 0.003	0.788 0.772	0.786 0.774	0.311	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.511 0.501	0.210 0.170	0.067 0.057	0.815 0.805	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B4					03/12/2013

Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2021/12/29	V1.0	Product Datasheet Creation
2021/01/14	V1.1	Modify according to the new matching topology
2025/6/16	V2.0	Change the carrier application to 0.4-3GHz 100W

Application data based on: YHG-21-20/22-01/TC-25-25

Notice