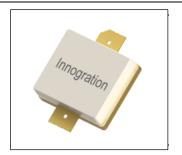
ITIV01400A2C LDMOS TRANSISTOR

400W, 50V High Power RF LDMOS FETs

Description

The ITIV01400A2C is a 400-watt capable, high performance, unmatched LDMOS FET, designed for wide-band commercial and industrial applications with frequencies HF to 200MHz, in new generation highly cost effective open cavity package.

It is featured by single ended configuration for high power and high ruggedness, suitable for Industrial, Scientific and Medical application



Typical 40.68MHz performance at different Vds bias(on Innogration test board with device soldered)
 Signal: CW ,,Idq=100mA

Voltage	Psat	Psat	Ids	Pin	Gain	Eff	2nd
(V)	(dBm)	(W)	(A)	(dBm)	(dB)	(%)	(dBc)
50	56.2	420	10.5	32.2	24	80.11	-31.5
28	51.57	143.5	6.55	28.62	22.95	78.27	-31.5
20	48.8	75.9	4.75	27.66	21.14	79.85	-31.5
15	46.18	41.5	3.5	25.78	20.4	79.04	-31.5
12	44.25	26.6	2.79	25.78	18.47	79.47	-31.5

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 136-174MHz (Commercial ground communication)
- Laser Exciter
- Synchrotron
- MRI
- · Plasma generator
- · Weather Radar

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
DrainSource Voltage	V _{DSS}	+160	Vdc
GateSource Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	Tc	+150	°C
Operating Junction Temperature	TJ	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case	D	0.5	0000
T _C = 85°C, T _J =200°C, DC test	R⊕JC	0.5	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22A114)	Class 2

Characteristic	Symbol	Min	Тур	Max	Unit
DC Characteristics (per half section)					
Drain-Source Voltage	V		160		V
V _{GS} =0, I _{DS} =1.0mA	$V_{(BR)DSS}$		100		V
Zero Gate Voltage Drain Leakage Current				1	^
$(V_{DS} = 75V, V_{GS} = 0 V)$	I _{DSS}	<u>——</u>	<u>——</u>	'	μΑ
Zero Gate Voltage Drain Leakage Current				1	^
$(V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V})$	I _{DSS}		<u> </u>	'	μΑ
GateSource Leakage Current				1	μА
$(V_{GS} = 10 \text{ V}, V_{DS} = 0 \text{ V})$	I _{GSS}				
Gate Threshold Voltage	V (41)		2.65		V
$(V_{DS} = 50V, I_D = 600 \mu A)$	V _{GS} (th)		2.00		V
Gate Quiescent Voltage	V		3.6		V
(V _{DD} = 50 V, I _D = 300 mA, Measured in Functional Test)	$V_{GS(Q)}$		5.0		V

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 50 Vdc, I_{DQ} = 100 mA, f =100MHz, pulse width:100us, duty cycle:10%

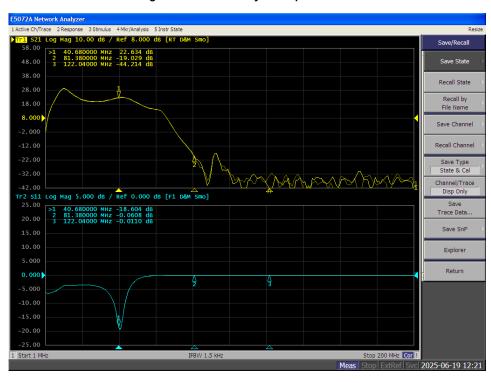
Load 65:1 All phase angles, at 400W Pulsed CW Output Power

No Device Degradation

40.68MHz

TYPICAL CHARACTERISTICS

Figure 1: Network analyzer output S11/S21



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Reference Circuit of Test Fixture Assembly Diagram

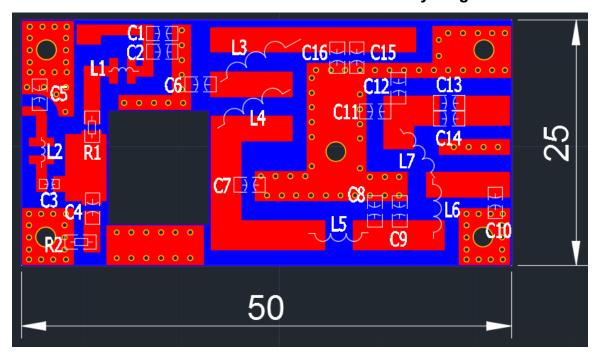
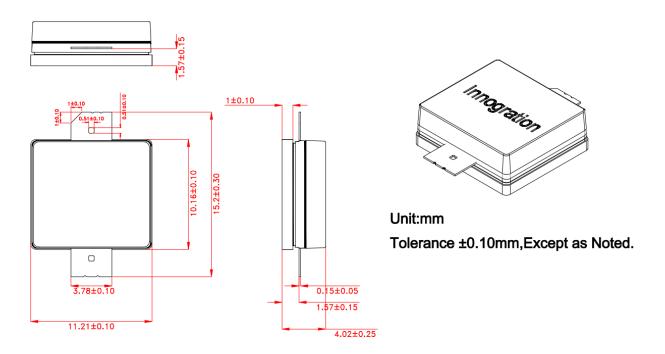


Table 5. Test Circuit Component Designations and Values

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C1,C4,C15	10uF/1210	1		
C2,C3	10nF/0805			
C5	270pF/MQ301111			
C6	47pF//MQ301111			
C7	120pF/MQ301111			
C8	150pF/MQ301111			
C9	270pF/MQ301111 +10pF/MQ301111			
C10	20pF/MQ301111			
C11	56pF/MQ301111			
C12	8.2pF/MQ301111			
C13,C14,C16	1000pF/MQ301111			
R1	240Ω/1206	1		

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Package Dimensions (Unit:mm)



Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2025/6/20	Rev 1.0	Advanced Datasheet Creation

Application data based on SJJ-25-16

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