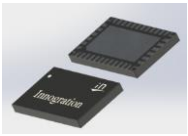
55W,12.5V High Power RF LDMOS FETs

ITGH09180RC6



Description

The ITGH09180RC6 is a 55-watt, highly rugged, input matched LDMOS FET, designed for commercial and industrial applications at frequencies up to 520MHz. It can be used in linear or saturated power amplifier, for CW and pulsed signal, and any modulation format. It is also featured by its lower cost of plastic open cavity for surface mount on PCB through high density vias

- Typical UHF CW Performance at 520M with different bias(On Innogration fixture with device soldered).Idq=20mA

Voltage (V)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
12.5	46.74	47.2	61.6	14.26	47.44	55.5	65
13.6	47.32	53.9	60.7	14.51	48.02	63.4	64

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- HF to UHF Land mobile radio (LMR)
- ISM applications

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+65	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+24	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	$R_{\theta JC}$	0.45	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage	$V_{(BR)DSS}$		65		V

V_{GS}=0, I_{DS}=100uA					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 13.6V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate--Source Leakage Current (V_{GS} = 9 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 13.6V, I_D = 600 μA)	$V_{GS(th)}$	——	2	——	V
Gate Quiescent Voltage (V_{DD} = 13.6V, I_D = 100mA, Measured in Functional Test)	$V_{GS(Q)}$	——	2.8	——	V

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 13.6Vdc, I_{DQ} = 10 mA, f = 520 MHz

VSWR 10:1 at 55W pulse CW Output Power	No Device Degradation

Figure 1:Pin Definition(Top View)

Pin No.	Symbol	Description
1-7,12,13,18-25,30,31,36	GND	DC/RF Ground
8,9,10,11,14,15,16,17	Vgs/RF In	Vgs and RF input
26,27,28,29,32,33,34,35	Vds/RF out	Vds and RF output
Package Base	GND	DC/RF Ground.

Reference Circuit of Test Fixture Assembly Diagram
520MHz RO4350B 20mils

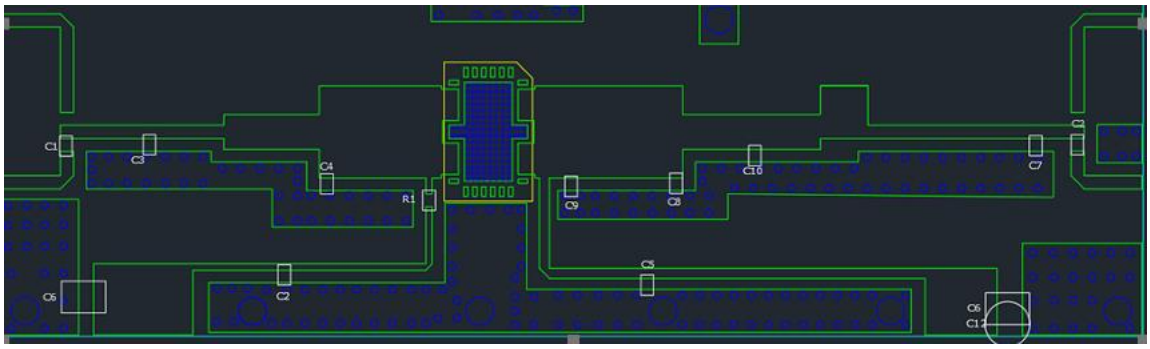


Figure 5. Test Circuit Component Layout

Table 5. Test Circuit Component Designations and Values

Component	Value	Quantity
C1	3.9pF	1
C2	220pF	2
R1	10 ohm	1
C3	20pF	1
C4	6.8pF	1
C5	100pF	1
C6	10uF	2
C7	0.5pF	1
C8	8.2pF	1
C9	18pF	1
C12	470uF	1
C10	30pF	1

Figure 1: Network analyzer Output S21/S11

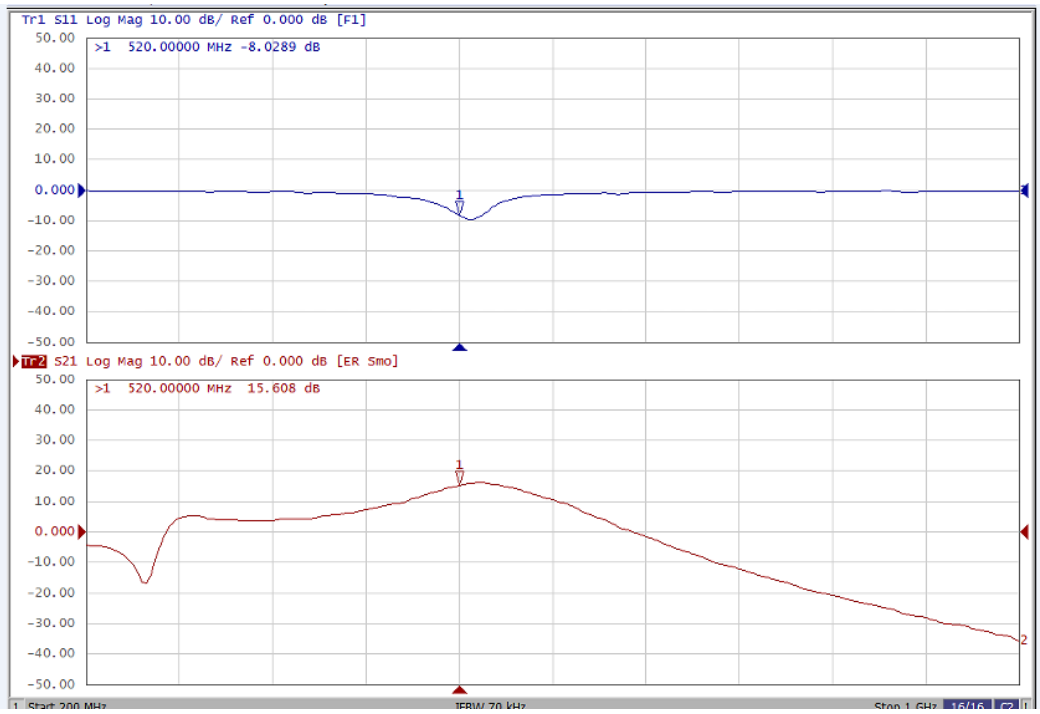
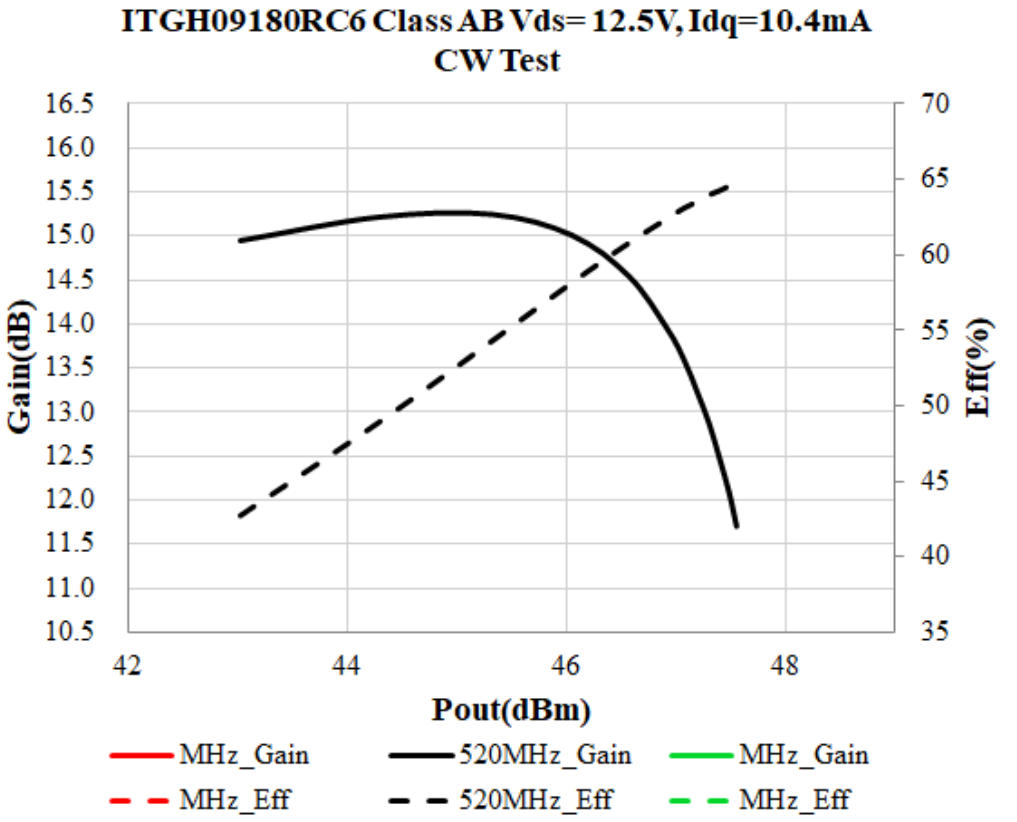
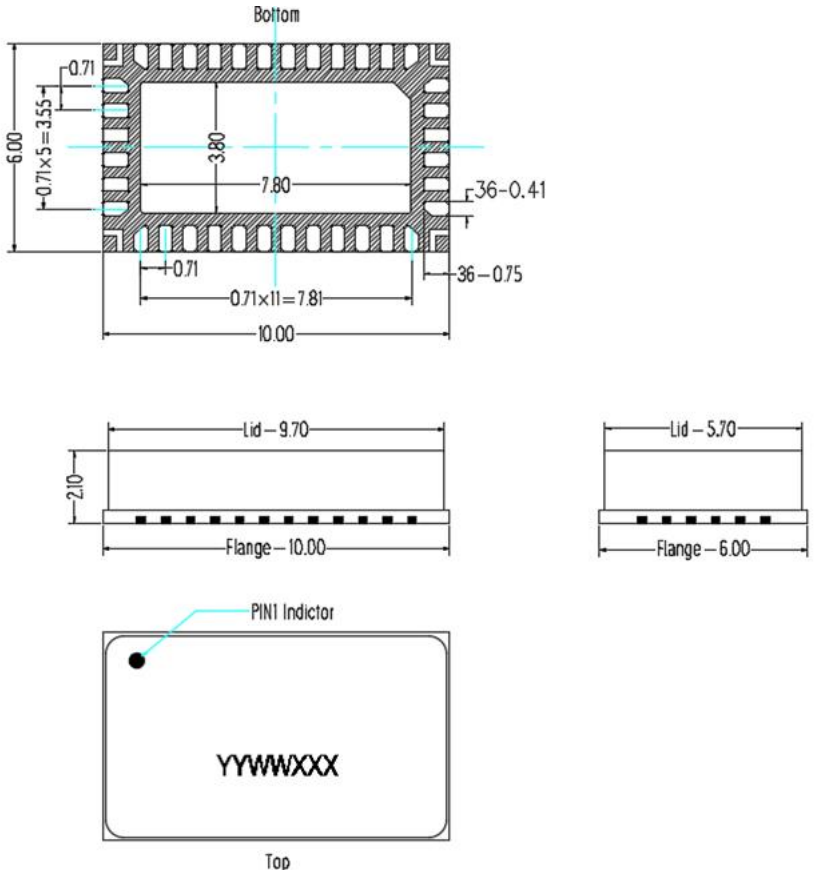


Figure 2: CW output power gain and efficiency as function of Pout



Package Dimensions

10*6 Plastic Package



Notes:

1. All dimensions are in mm;
2. The tolerances unless specified are ±0.2mm.

Revision history

Table 7. Document revision history

Date	Revision	Datasheet Status
2025/6/30	**Rev 1.0**	**Preliminary Datasheet**

Application data based on ZXY-25-7

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