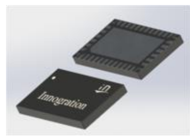
GaN HEMT 50V, 100W, 5.9-6.5GHz Power Transistor

STAV65100C6



Description

The STAV65100C6 is a dual path 100W, internal matched GaN HEMT, operated from 5.9-6.5GHz.

It features high gain, high efficiency, wide band and low cost, in 10*6mm open cavity plastic package.

It can be configured as a single stage Doherty capable of delivering Pavg of 14W.

There is no guarantee of performance when this part is used outside of stated frequencies.

It is recommended to use copper coin underneath the transistor for best heat dissipation.

- Typical Doherty Single--Carrier W--CDMA Characterization Performance:

V_{DS}= 50V, $I_{DQ-Mian}$=80 mA Vgs-main=-3.07V. Vgs-peak=-5.20V, 1 carrier WCDMA

Freq (MHz)	Pout (dBm)	ACPR (dBc)	Gain (dB)	Efficiency (%)
5900		-30.85	10.19	43.01
6000		-38.30	10.41	41.19
6100		-35.20	10.81	38.87
6200	42	-32.19	10.55	36.50
6300		-32.25	10.59	35.60
6400		-34.21	10.34	35.96
6500		-36.12	9.95	36.90

Applications

- 5G advanced power amplifier
- C band power amplifier

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

Turning the device ON

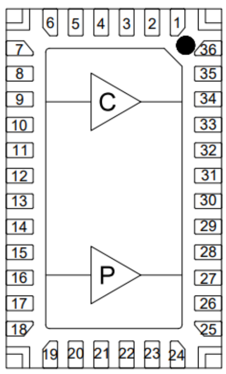
1. Set VGS to the pinch--off (VP) voltage, typically –5 V
2. Turn on VDS to nominal supply voltage
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically –5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

Figure 1: Pin Connection definition

Transparent top view (Backside grounding for source)



Pin No.	Symbol	Description
8,9,10,11	RF IN/Vgs1	RF Input, Vgs bias for carrier path
32,33,34,35	RF OUT/VDD1	RF Output, VDD bias for carrier path
14,15,16,17	RF IN/Vgs2	RF Input, Vgs bias for peak path
26,27,28,29	RF OUT/VDD2	RF Output, VDD bias for peak path
Rest pins	NC	No connection
2,5,7,12,13,18,20,23,25,30,31,36, Package Base	GND	DC/RF Ground. Must be soldered directly to heatsink or copper coin for CW application.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+200	Vdc
Gate--Source Voltage	V_{GS}	-8 to +0.5	Vdc
Operating Voltage	V_{DD}	55	Vdc
Maximum gate current	Igs	13	mA
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case by FEA T_C= 85°C, Pdiss=30W at Pavg=42dBm WCDMA 1 carrier	$R_{\theta JC}$	TBD	°C /W

Notes: Based on expected carrier amplifier efficiency of Doherty, Pavg assumes 10% peaking amplifier contribution of total average Doherty rated power. Thermal resistance is measured to package backside

Table 3. Electrical Characteristics (TA = 25℃ unless otherwise noted)

DC Characteristics (main path, measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	VGS=-8V; IDS=5mA	V_{DSS}		200		V
Gate Threshold Voltage	VDS =10V, ID = 5mA	$V_{GS(th)}$	-4	-3.2	-2	V
Gate Quiescent Voltage	VDS =50V, IDS=55mA, Measured in Functional Test	$V_{GS(Q)}$		-3		V

DC Characteristics (peak path, measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	VGS=-8V; IDS=8mA	V_{DSS}		200		V
Gate Threshold Voltage	VDS =10V, ID = 8mA	$V_{GS(th)}$	-4	-3.1	-2	V
Gate Quiescent Voltage	VDS =50V, IDS=60mA, Measured in Functional Test	$V_{GS(Q)}$		-3		V

Ruggedness Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Load mismatch capability	6GHz, Pout=42dBm WCDMA 1 Carrier, All phase, No device damages	VSWR		10:1		

Figure 2: Efficiency and power gain as function of Pout

(VDD = 50 Vdc, IDQ = 80 mA, Pulse width=20us, duty cycle=20%)

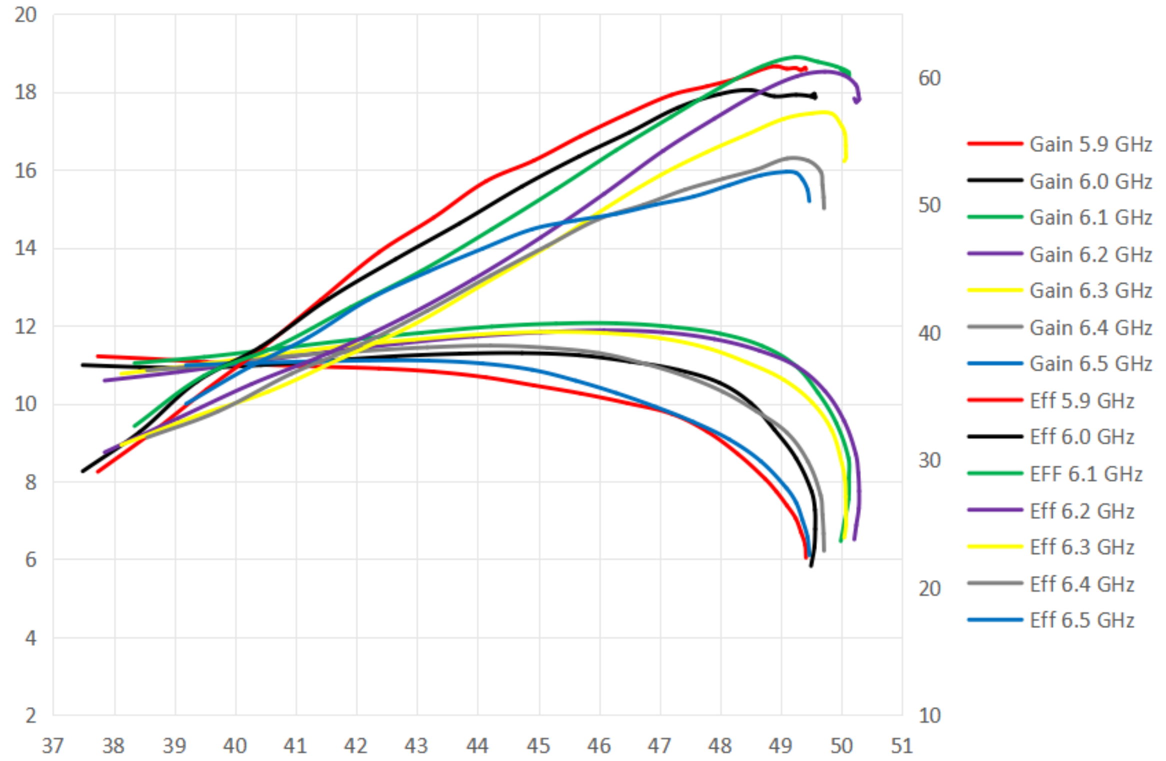
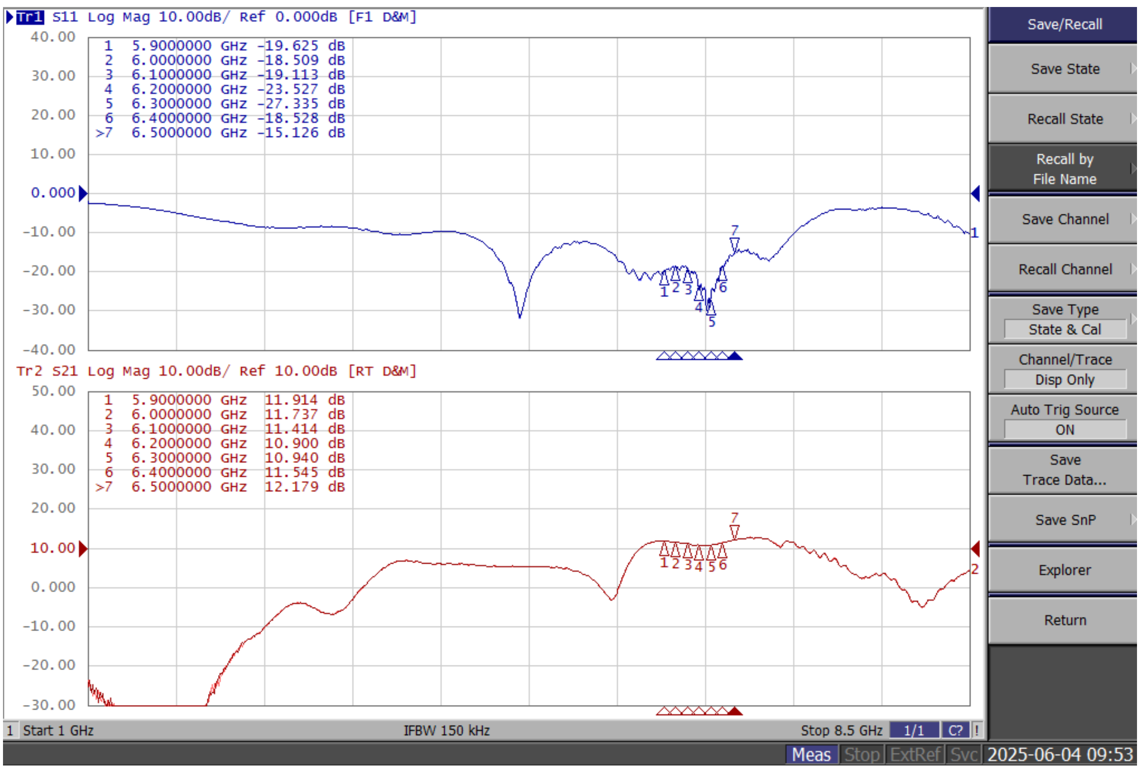
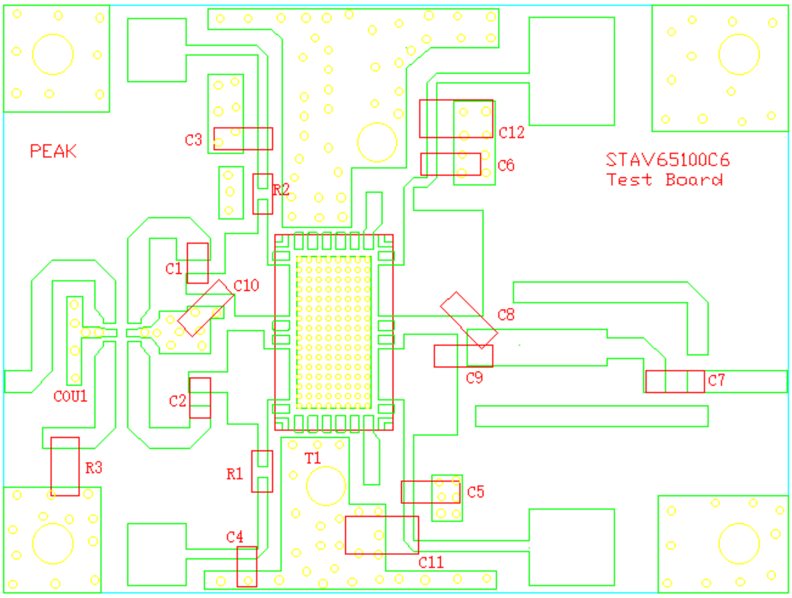


Figure 3: S11/S21 output from Network analyser

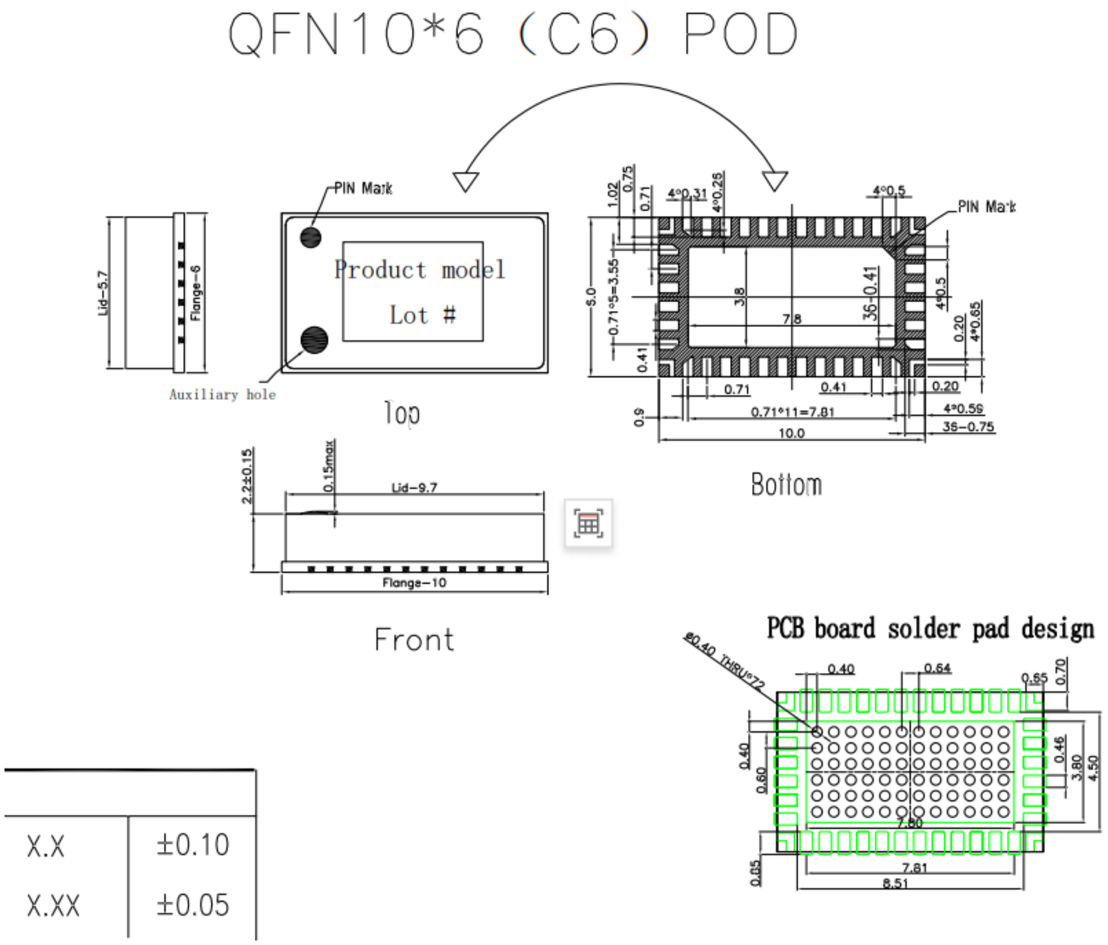




Part	Quantity	Description	Part Number	Manufacture
C1,C2,C3,C4,C5,C6,C7	7	2.0pFHigh Q Capacitor	251SHS2R0BSE	TEMEX
C11,C12	2	10uF MLCC	GRM32EC72A106ME05	Murata
C9	1	0.8pFHigh Q Capacitor	251SHS0R8BSE	TEMEX
C8	1	8.2pFHigh Q Capacitor	251SHS8R2BSE	TEMEX
C10	1	0.3pFHigh Q Capacitor	251SHS0R3BSE	TEMEX
COU1	1	3 dB Bridge	C5060J5003AHF	ANAREN
R1,R2	1	10Ω Power Resistor	ESR03EZPF100	ROHM
R3	1	51Ω Power Resistor	1206	ROHM
T1	1	GaN Transistor	STAV65100C6	Innogration

Package Dimensions

10*6 Plastic Package



Notes:

1. All dimensions are in mm;
2. The tolerances unless specified are ±0.2mm.

Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2025/6/4	V1.0	Preliminary Datasheet Creation

Application data based on: LWH-25-21

Notice