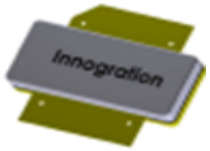
STCV07850RC2 LDMOS TRANSISTOR

Document Number: STCV07850RC2
Preliminary Datasheet V1.0

850W ,50V UHF/VHF CW RF Power Transistor

STCV07850RC2



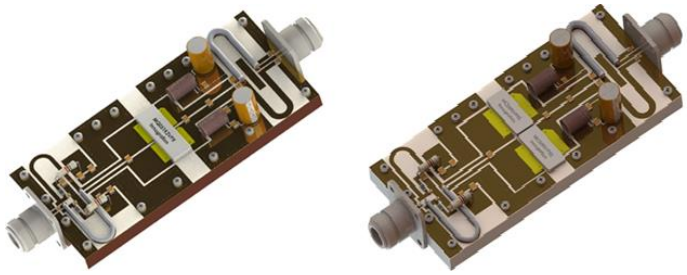
Description

The STCV07850RC2 itself is a 850-watt capable, high performance, internal match，single ended GaN HEMT transistor，idea for RF Energy and ISM application at fixed frequency point or very narrow band below 700MHz, typically for 650MHz or 433MHz applications.

There is no guarantee of performance when this part is used outside of stated frequencies.

It is recommended to use paired STCV07850RC2 to enable about1600W designed for ISM application. Compared to similar power level but in single dual-path packaged device, it offers better thermal management and easier maintenance.

Demonstration of paired STCV07850RC2(right) Vs single dual-path device(left) at 650MHz



- Typical performance(on 650MHz narrow band application board with **STCV07850RC2** devices soldered)

V_{DS}=50V,Vgs=-4.2V, CW,

V_{DS} (V)	Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
48	650	57.78	600.0	70.6	17.08	59.02	797.9	79.8
50	650	58.28	672.6	71.9	17.09	59.42	875.0	80.4

Applications

- P band amplifier
- UHF/VHF PA

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

Turning the device ON

1. Set VGS to the pinch--off (VP) voltage, typically –5 V
2. Turn on VDS to nominal supply voltage
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically –5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+200	Vdc
Gate--Source Voltage	V_{GS}	-8 to +0.5	Vdc
Operating Voltage	V_{DD}	55	Vdc
Maximum gate current	Igs	100	mA
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C

Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case by FEA T_C= 25°C, at Pd=210W	$R_{\theta JC}$	0.55	°C /W

Table 3. Electrical Characteristics (TA = 25℃ unless otherwise noted)

DC Characteristics (Each path, measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	VGS=-8V; IDS=140.4mA	V_{DSS}		200		V
Gate Threshold Voltage	VDS =10V, ID = 140.4mA	$V_{GS(th)}$	-4	-	-2	V
Gate Quiescent Voltage	VDS =50V, IDS=600mA, Measured in Functional Test	$V_{GS(Q)}$		--3.1		V

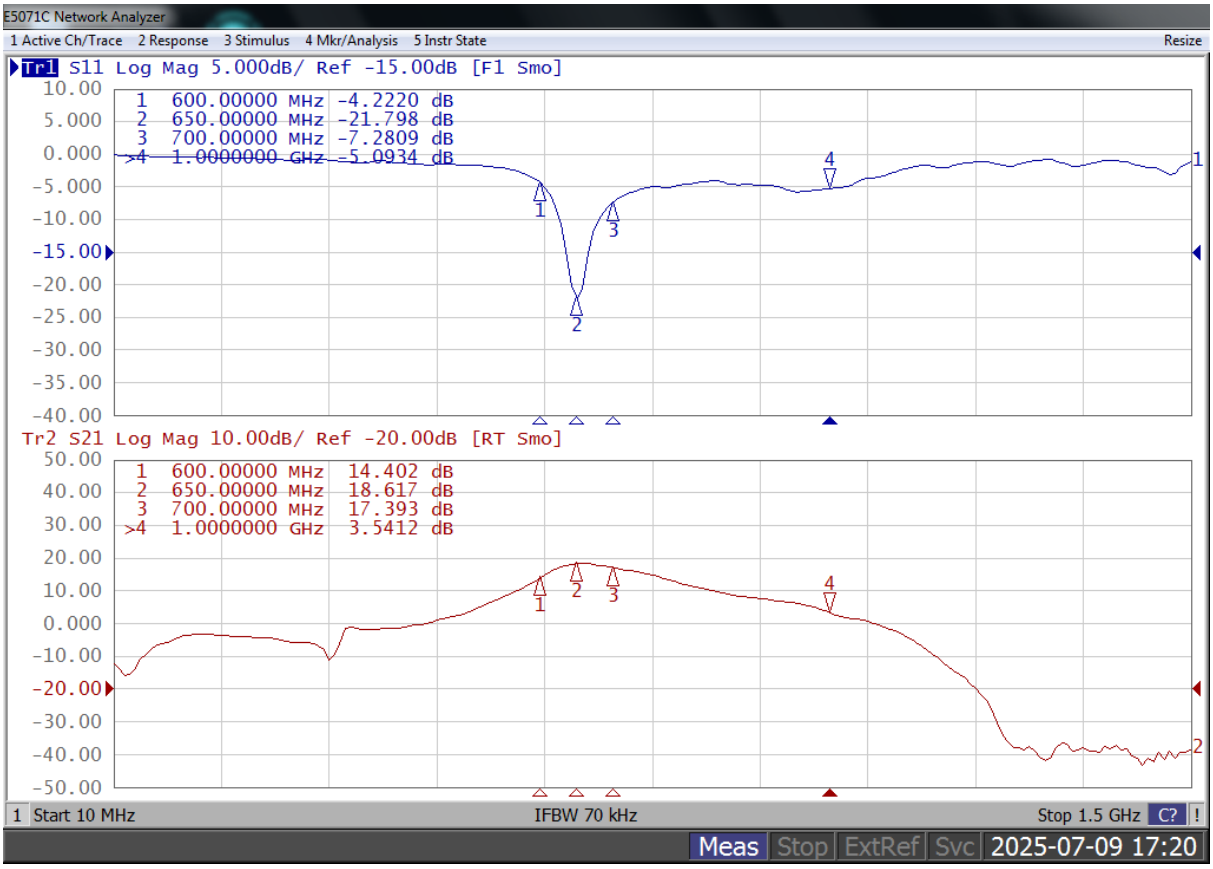
Ruggedness Characteristics in Paired configurations

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Load mismatch capability	0.7GHz, Pout=850W pulse CW All phase, No device damages	VSWR		5:1		

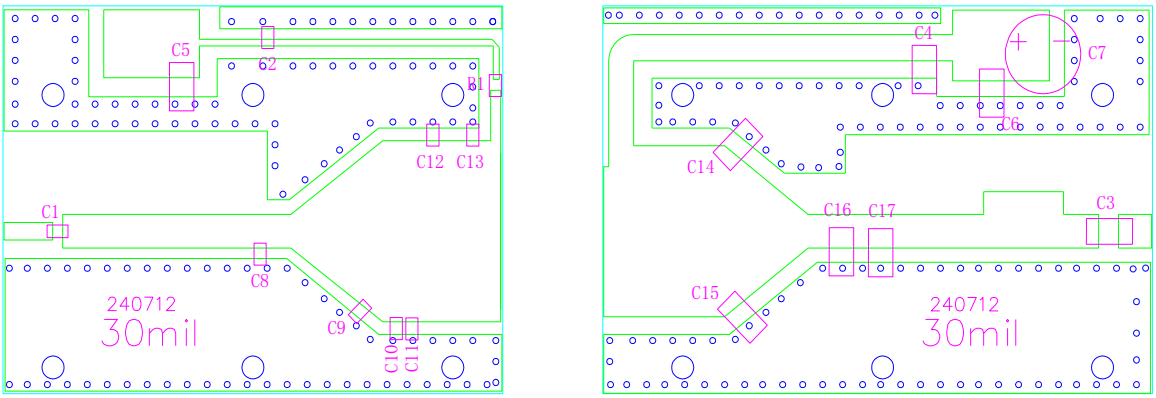
TYPICAL CHARACTERISTICS

STCV07850RC2 at 650MHz

Figure 1: Network analyzer output S11/S21 Vds=50V, Idq=600mA，Pin=0dBm



Reference Circuit of Test Fixture

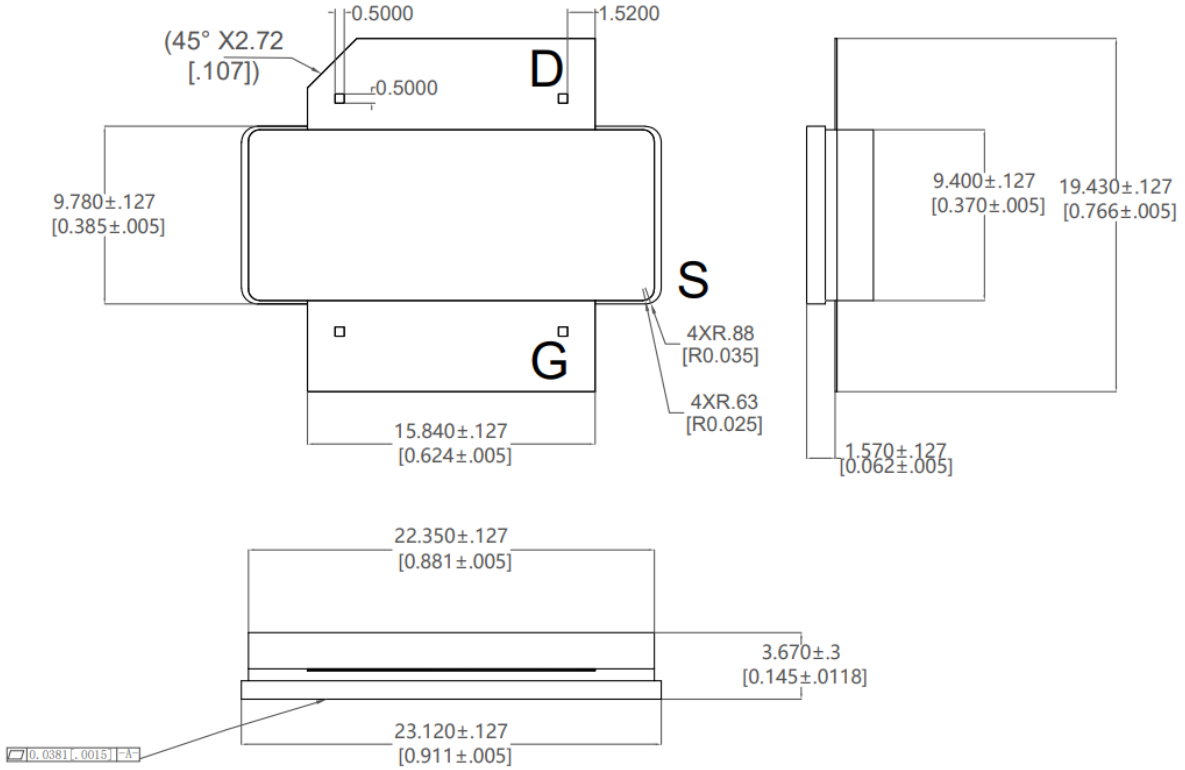


Designator	Footprint	Comment	Quantity
C1	0603/0805	4.7pF	1
C2	0603/0805	82pF	1
C3	1210	27pF*3	3
C4	1210	82pF	1
C5, C6	1210	10 uF/100V	2
C7		1000 uF/63V	1
C8, C9, C10, C11	0603/0805	10 pF	4
C12	0603/0805	6.8 pF	1
C13	0603/0805	15 pF	4
C14, C15, C16, C17	1210	10 pF	4

Package Outline

Flangeless ceramic package;

INP-688-2-EL（C2)



OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-C2					09/27/2018

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2025/6/20	Rev 1.0	Preliminary datasheet

Application data based on TC-25-17

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