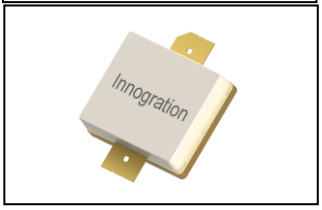
55W,12.5V High Power RF LDMOS FETs

ITGH09180RA2C



Description

The ITGH09180RA2C is a 55-watt, highly rugged, input matched LDMOS FET, designed for commercial and industrial applications at frequencies up to 520MHz. It can be used in linear or saturated power amplifier, for CW and pulsed signal, and any modulation format.

- Typical VHF CW Performance (On Innogration fixture with device soldered).

Vds=12.5V Idq=100mA

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
40.68	46.42	43.9	68.3	21.29	47.44	55.4	76.5

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- HF to UHF Land mobile radio (LMR)
- ISM applications

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+65	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+24	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	RθJC	0.40	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage V_{GS}=0, I_{DS}=100uA	$V_{(BR)DSS}$		65		V
Zero Gate Voltage Drain Leakage Current	I_{DSS}	——	——	1	μA

(V_{DS} = 13.6V, V_{GS} = 0 V)					
Gate--Source Leakage Current (V_{GS} = 9 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 13.6V, I_D = 600 μA)	$V_{GS(th)}$	——	2	——	V
Gate Quiescent Voltage (V_{DD} = 13.6V, I_D = 100mA, Measured in Functional Test)	$V_{GS(Q)}$	——	2.8	——	V

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 13.6Vdc, I_{DQ} = 100 mA, f = 520 MHz

VSWR 10:1 at 55W pulse CW Output Power	No Device Degradation

40.68MHz

Reference Circuit of Test Fixture Assembly Diagram

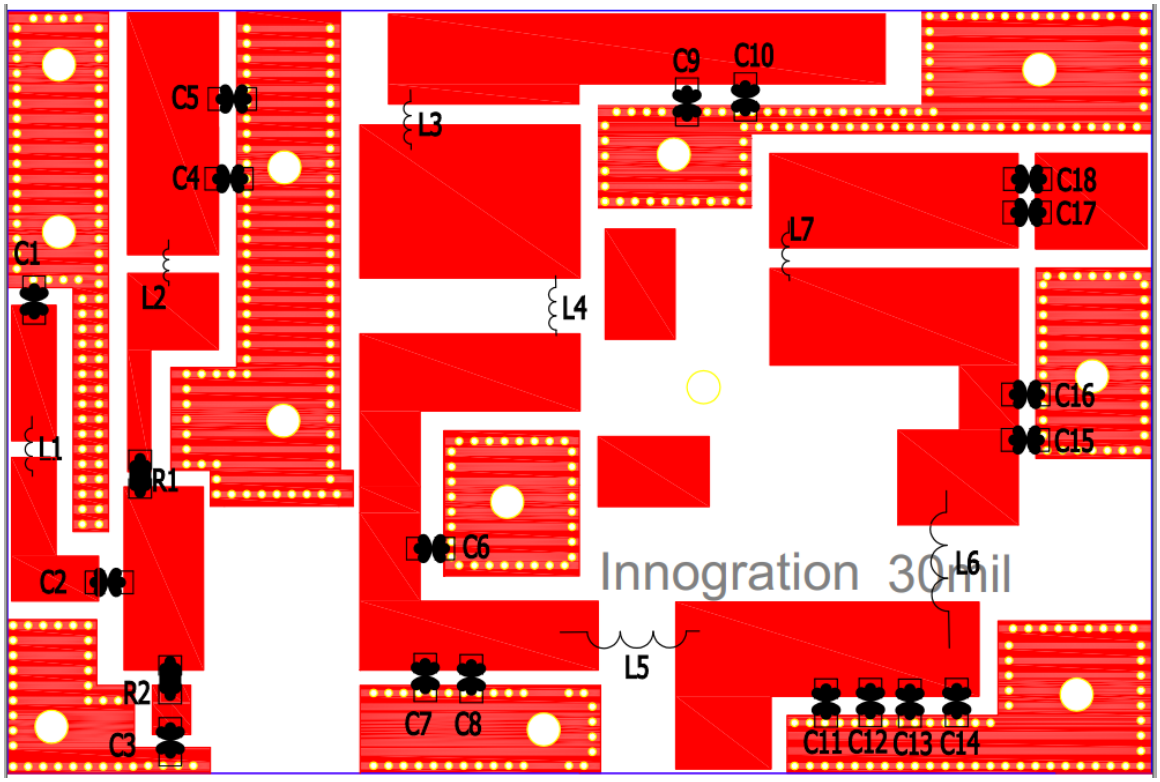


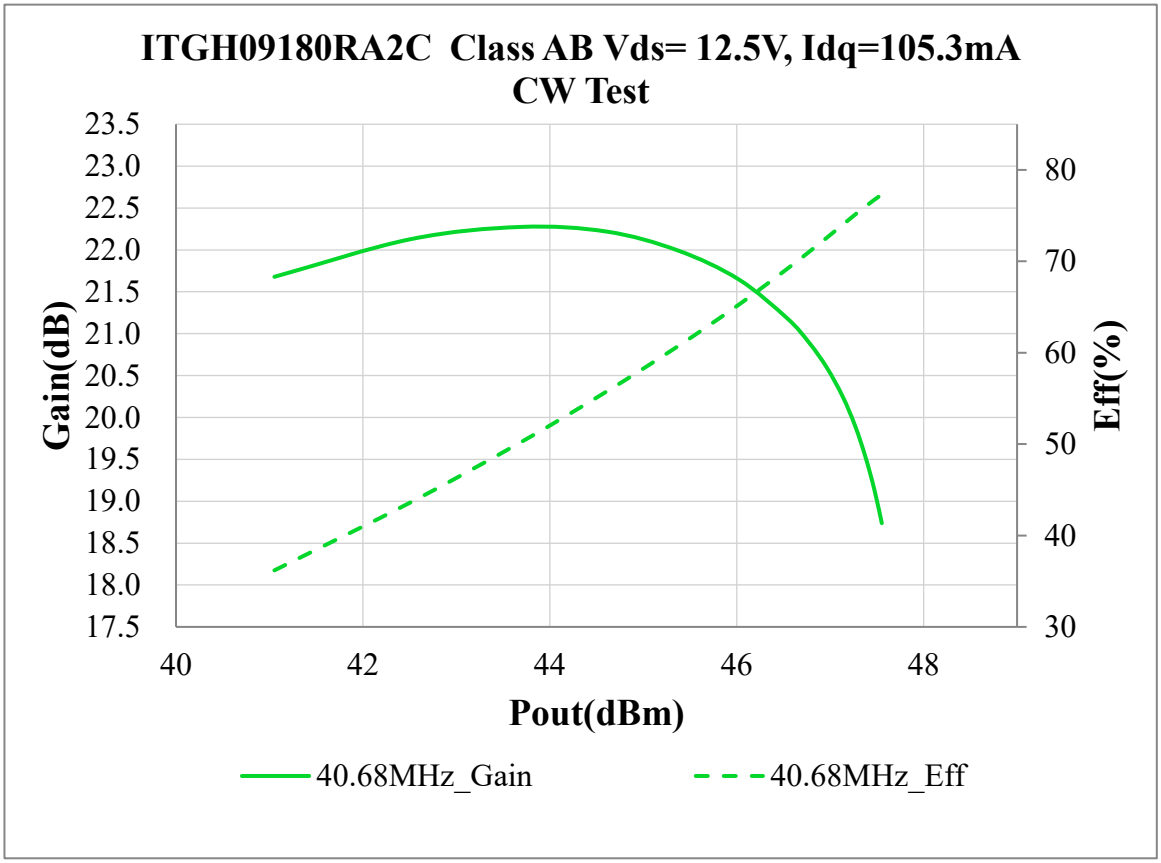
Figure 1. Test Circuit Component Layout

Table 5. Test Circuit Component Designations and Values

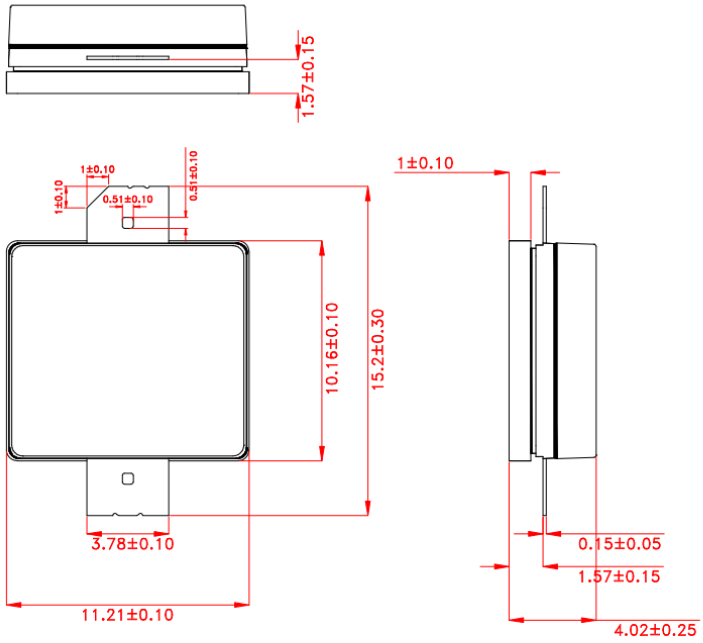
C3,C5,C10	10uF/1210	
C2,C4,C9,C17,C18	10nF/1210	
C1,C11,C12,C13	100pF/MQ301111	
C6,C7,C8	30pF//MQ301111	
C14	75pF/MQ301111	

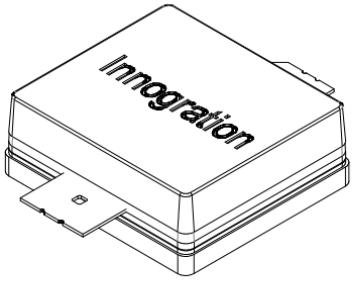
C15	56pF/MQ301111	
C16	12pF/MQ301111	
R1	300Ω/1206	
R2	11Ω/1206	
L1	150nH	
L2	160nH	
L3,L4	1.5mm wire，7 turns, ϕ=5mm	DIY
L5	1.5mm wire，3 turns, ϕ=5mm	DIY
L6	1.5mm wire，2 turns, ϕ=5mm	DIY
L7	1.5mm wire，7 turns, ϕ=5mm	DIY

Figure 2: CW output power gain and efficiency as function of Pout



Package Dimensions





Unit:mm

Tolerance ±0.10mm,Except as Noted.

Revision history

Table 7. Document revision history

Date	Revision	Datasheet Status
2025/7/1	Rev 1.0	Preliminary Datasheet

Application data based on LBG-25-26

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