

MV1536GR LDMOS TRANSISTOR

Document Number: MV1536GR
Preliminary Datasheet V1.0

100W, 12.5V High Power RF LDMOS FETs

Description

The MV1536GR is a 100-watt capable, high performance, unmatched LDMOS FET, designed for commercial and industrial applications with frequencies HF to 0.1 GHz.

MV1536GR



• Typical 30MHz Performance at different bias

CW, $V_{GS}=2.5V, I_{DQ}=300mA$					
Voltage(V)	Pin(dBm)	Pout(W)	Gain(dB)	EFF (%)	2 nd (dB)
12.5	32.6	105	17.6	70	-28
14.4	32.6	135	18.6	69	-28

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- 2-30MHz (HF or Short wave communication)
- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DS}	+65	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+24	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_c	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case $T_c=85^{\circ}C, T_J=200^{\circ}C, DC\ test$	$R_{\theta JC}$	0.24	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics ($T_A = 25^{\circ}C$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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DC Characteristics

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Drain-Source Voltage $V_{GS}=0, I_{DS}=1.0mA$	$V_{(BR)DSS}$	65	70		V
Zero Gate Voltage Drain Leakage Current $(V_{DS} = 28 V, V_{GS} = 0 V)$	I_{DSS}	—	—	1	μA
Gate--Source Leakage Current $(V_{GS} = 10 V, V_{DS} = 0 V)$	I_{GSS}	—	—	1	μA
Gate Threshold Voltage $(V_{DS} = 28V, I_D = 600 \mu A)$	$V_{GS(th)}$	—	1.98	—	V
Gate Quiescent Voltage $(V_{DD} = 28 V, I_D = 300 mA, \text{Measured in Functional Test})$	$V_{GS(Q)}$	—	2.5	—	V
Drain source on state resistance $(V_{DS} = 0.1V, V_{GS} = 10 V)$	$R_{ds(on)}$		35		m Ω
Common Source Input Capacitance $(V_{GS} = 0V, V_{DS} = 28 V, f = 1 MHz)$	C_{ISS}		250		pF
Common Source Output Capacitance $(V_{GS} = 0V, V_{DS} = 28 V, f = 1 MHz)$	C_{OSS}		110		pF
Common Source Feedback Capacitance $(V_{GS} = 0V, V_{DS} = 28 V, f = 1 MHz)$	C_{RSS}		6.6		pF

Load Mismatch (In Innogration Test Fixture, 50 ohm system): $V_{DD} = 12.5 Vdc, I_{DQ} = 300 mA, f = 100 MHz$

VSWR 20:1 at 100W Pulsed CW Output Power	No Device Degradation
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Pin definitions

1: Gate

2-4: Drain

Flange: source for grounding

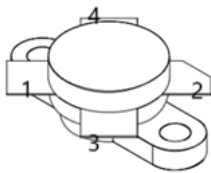


Figure 1: Network analyzer Output S11/S21

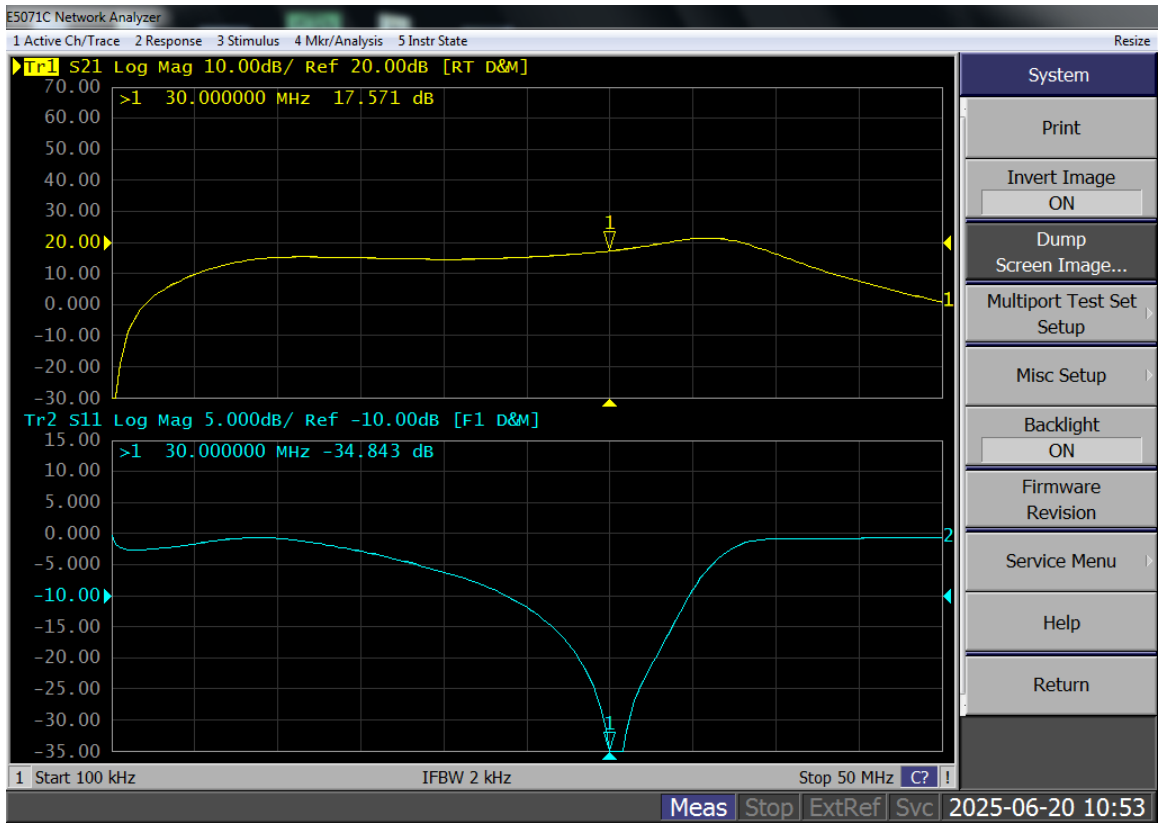
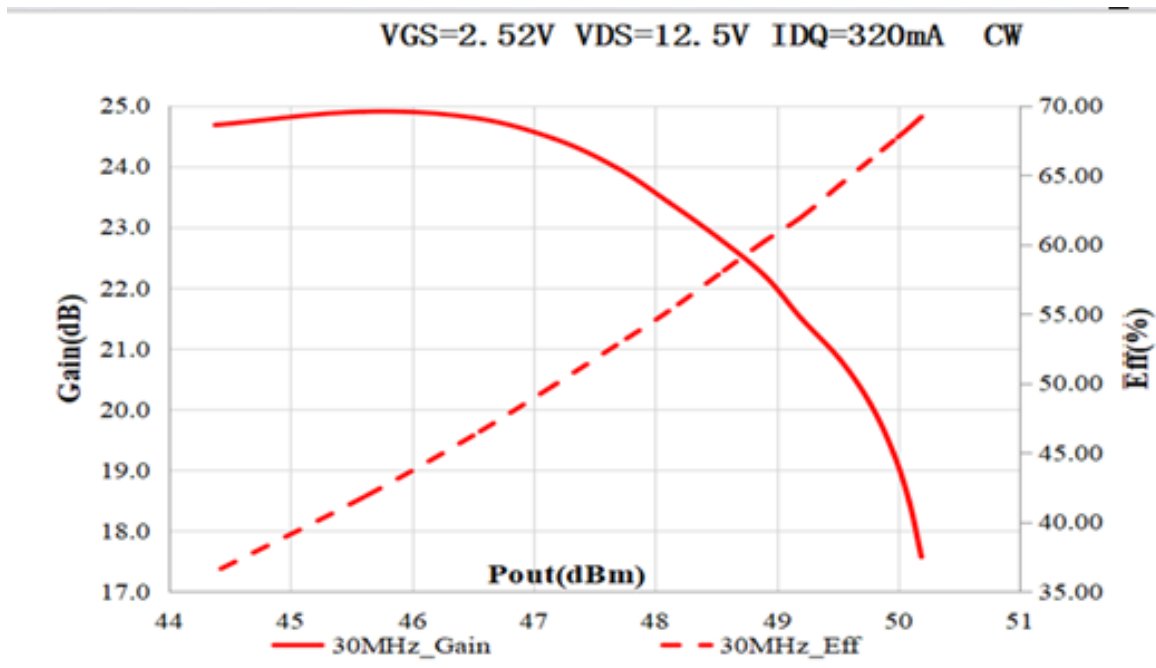
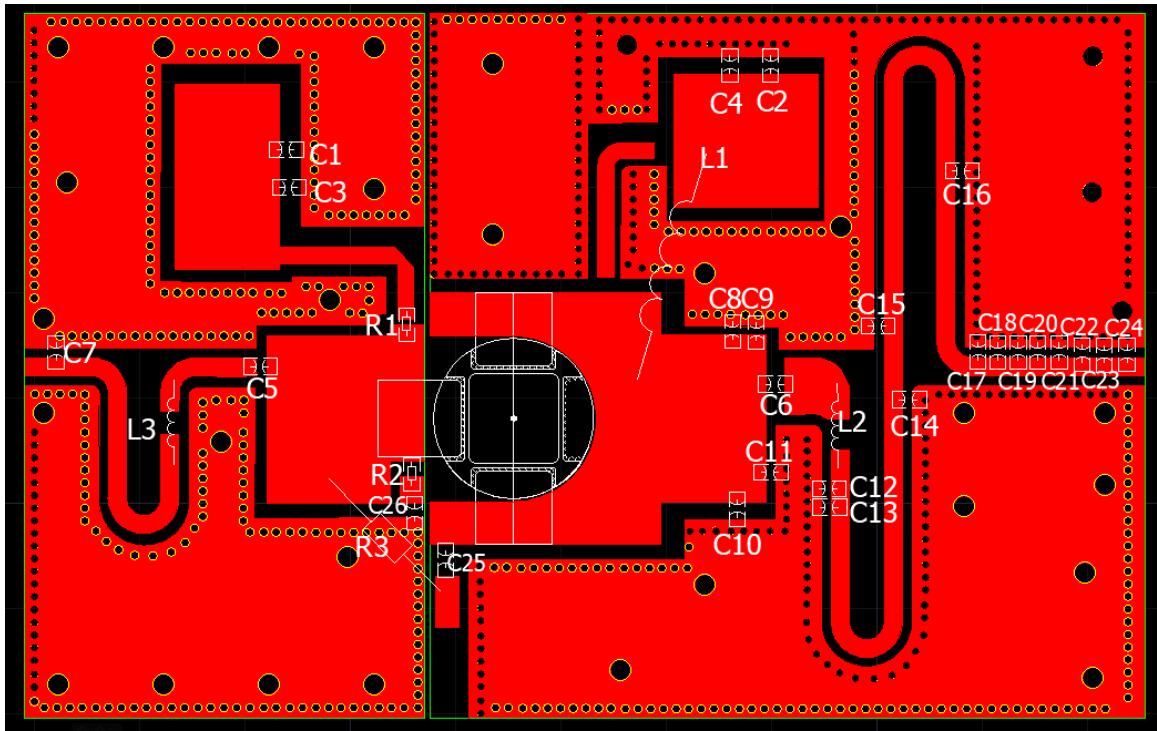


Figure 2: Power gain, Eff as function of Pout:



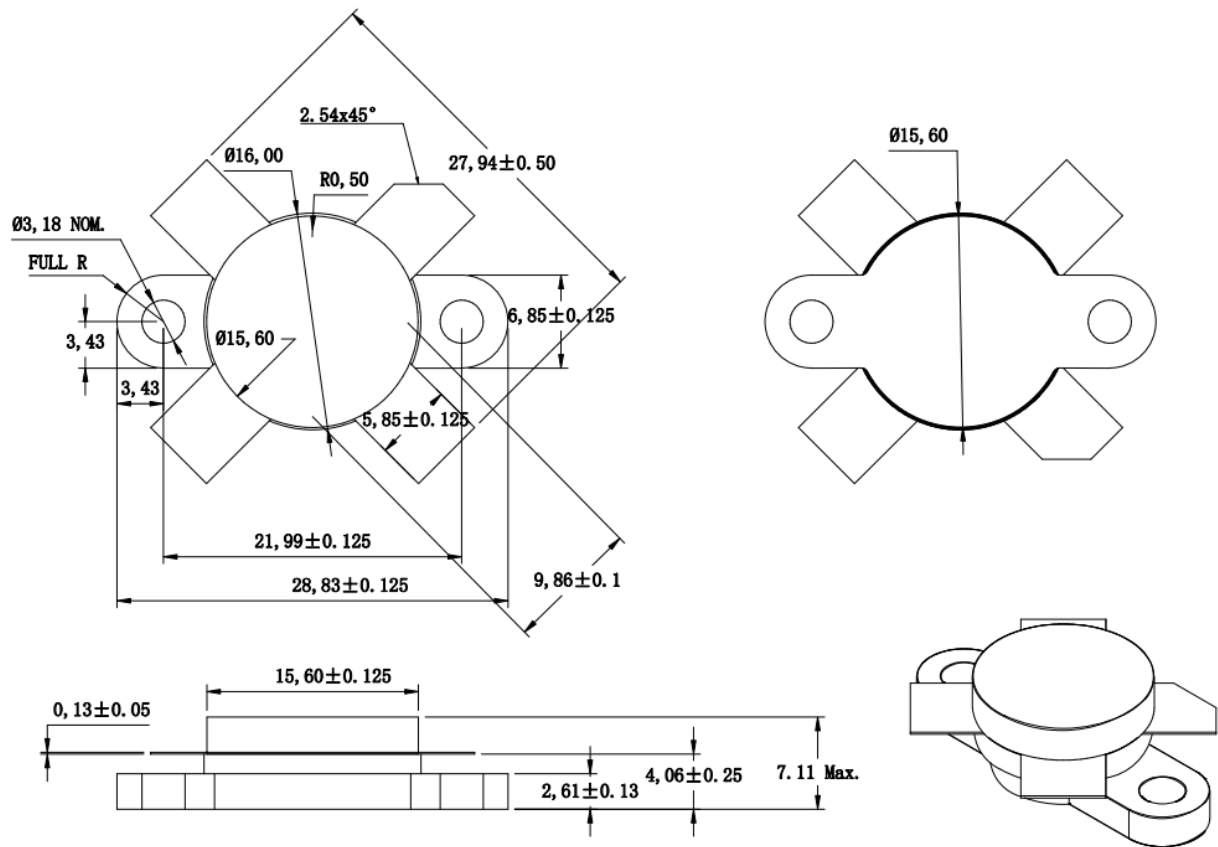
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Component	Description	Suggested Manufacturer
C1,C2,C25,C26	10uF/200V-1210	Ceramic multilayer capacitor
C3,C4,C5	10nF/200V-1210	Ceramic multilayer capacitor
C6	1000pF	
C7	240pF	
C8,C10,C13	47pF	
C9	200pF	
C11,C16,C24	100pF	
C12,C14,C18~C23	75pF	
C15	56F	
C17	160pF	
R1	10 Ω/1206	Chip Resistor
R2	51 Ω	Chip Resistor
R3	300 Ω	Color ring resistor
L1	1.5mm wire, 5mm innerdiameter, 14turns	DIY
L2	1.5mm wire, 5mm innerdiameter, 3turns	DIY
L3	1.5mm wire, 5mm innerdiameter, 7turns	DIY

Package Outline



Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2025/6/20	Rev 1.0	Preliminary Datasheet Creation

Application data based on TC-25-26

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