20W,28V L band broadband Plastic RF LDMOS

ITCH17W020P3

Description

The ITCH17W020P3 is a 20-watt, highly broadband, LDMOS transistor, in 6*5mm DFN plastic package, supporting surface mounted on PCB through high density grounding vias. Within 1-1.7GHz, it can deliver >20W CW with high performance

- Typical broadband Class AB RF Performance (On Innogration fixture with device soldered)

Vds=28V, Idq=100mA, CW

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
1000	43.15	20.7	61.7	15.23	43.97	25.0	65.0
1100	43.27	21.2	55.3	15.56	44.17	26.1	58.5
1200	43.69	23.4	50.8	15.51	44.57	28.6	54.0
1300	43.78	23.9	50.7	15.96	44.64	29.1	53.2
1400	43.76	23.8	52.0	16.16	44.67	29.3	54.6
1500	43.59	22.9	51.7	16.07	44.54	28.4	54.3
1600	43.37	21.7	51.3	15.95	44.28	26.8	53.3
1700	42.99	19.9	50.7	15.44	43.9	24.5	52.2

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+65	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+28	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, Pout=20W 1.7GHz	RθJC	0.9	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit

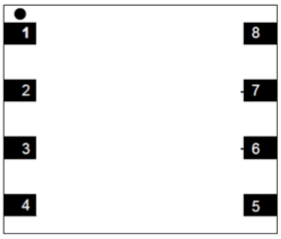
DC Characteristics

Drain-Source Voltage V_{GS}=0, I_{DS}=100uA	$V_{(BR)DSS}$		65		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate--Source Leakage Current (V_{GS} = 11 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 28V, I_D = 600 μA)	V_{GS}(th)	——	2	——	V
Gate Quiescent Voltage (V_{DD} = 28V, I_D = 100mA, Measured in Functional Test)	$V_{GS(Q)}$	——	2.8	——	V

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 28Vdc, I_{DQ} = 100 mA, f = 2100 MHz

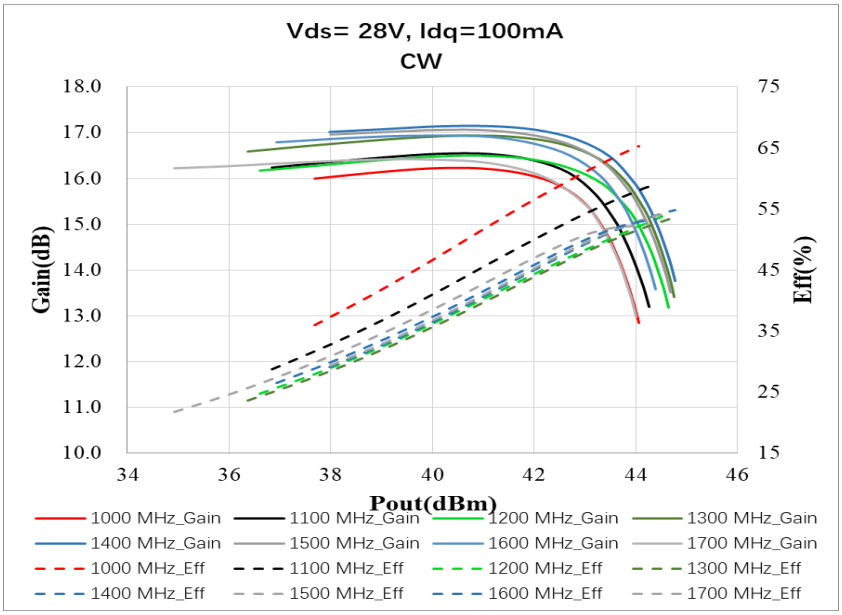
VSWR 10:1 at 10W pulse CW Output Power	No Device Degradation

Pin Configuration and Description(Top view)



Pin No.	Symbol	Description
1,2,3,4	RF IN/VGS	Gate Bias/RF Input
5,6, 7,8	RF OUT /VDS	RF Output, Drain Bias
Backside metal	GND	DC/RF Ground. Must be soldered to EVB ground plane over array of vias for thermal and RF performance. Solder voids under Pkg Base will result in excessive junction temperatures causing permanent damage.

Typical performance



Reference Circuit of Test Fixture Assembly Diagram
RO4350B 20mils

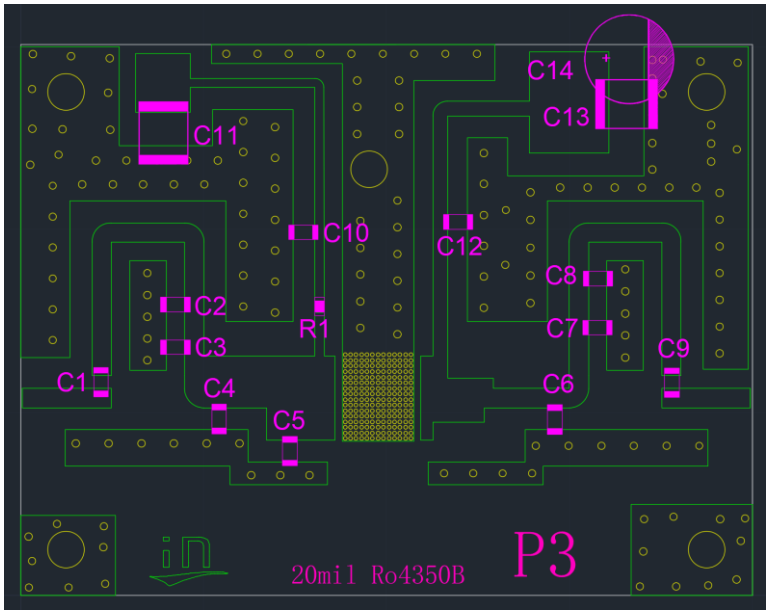
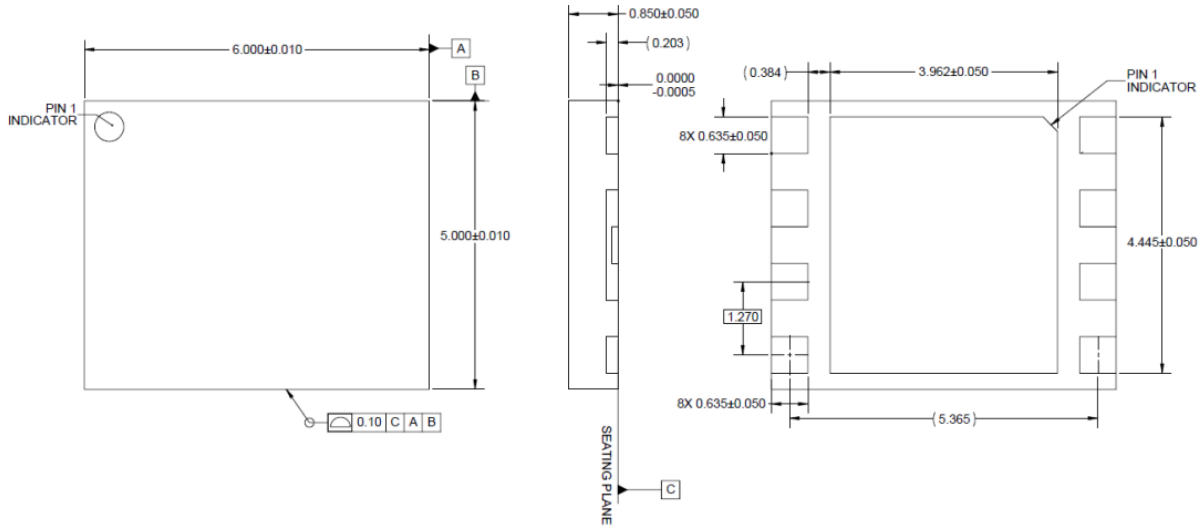


Figure 2. Test Circuit Component Layout

Reference	Footprint	Value	Quantity
C1,C9,C10,C12	0603	20 pF	4
C2,C8	0603	1 pF	2
C3	0603	2.7 pF	1
C4,C5	0603	3.9 pF	2
C6	0603	2.4 pF	1
C7	0603	1.8 pF	1
C11,C13	1210	10 uF/63V	2
C14	\	470 uF/63V	1
R1	0603	10 ohm	1
U1	P3	ITCH17W020P3	1

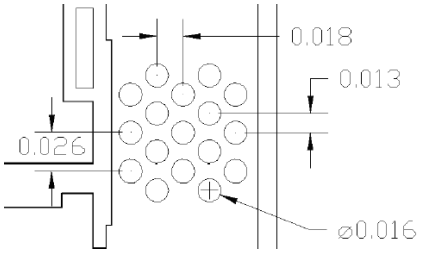
Package

6*5 DFN Package



Notes:
1. All dimensions are in mm. Otherwise noted, the tolerance is ±0.1 mm.
2. Package leads are gold plated.
3. Part is mold encapsulated.

Recommended vias layout: (all in inches)



Revision history

Table 7. Document revision history

Date	Revision	Datasheet Status
2025/7/21	Rev 1.0	Preliminary Datasheet

Application based on CWZ-25-12

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