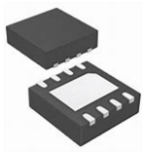
Gallium Nitride 28V 10W, RF Power Transistor

XTAH80010PD



DFN 4*4mm

Description

The XTAH80010PD is a 10W unmatched GaN HEMT, designed for multiple applications, up to 8000MHz. The transistor is available in a cost effective 4mm*4mm, surface mount, DFN package with 100% DC production test to ensure the quality and consistency.It can be used in CW, Pulse and multiple modulation mode.

- Typical Performance of class AB circuit (On different Innogration fixtures):

V_{DD} =28 V, I_{DQ} =30 mA, CW

Freq (MHz)	CW Signal			
	P_{1dB} (W)	Gain@ P_{1dB} (dB)	P_{3dB} (W)	η_D@P_3 (%)
5100-5900	10	10	13	57
6900-7200	8	10	11	50
7200-7800	8	8	11	47

Typical Performance of class AB circuit (On different Innogration fixtures):

V_{DD} =28 V, I_{DQ} =30 mA, WCDMA 1 carrier CCDF=10dB

Freq (MHz)	Pout=31dBm			
	CCDF (dB)	ACPR (dB)	Gain (dB)	η_D (%)
5100-5900	9.7	-40	11	20
7200-7800	9.5	-35	8	18

Recommended driver：GTAH80004PD

Applications and Features

- Suitable for wireless communication infrastructure, wideband amplifier, EMC testing, ISM etc.
- High Efficiency and Linear Gain Operations
- Thermally Enhanced Industry Standard Package
- High Reliability Metallization Process
- Excellent thermal Stability and Excellent Ruggedness
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

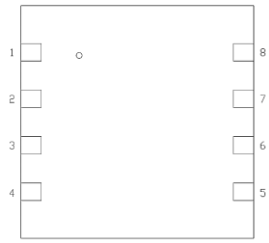
Turning the device ON

1. Set VGS to the pinch--off (VP) voltage, typically –5 V
2. Turn on VDS to nominal supply voltage (28V)
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically –5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

Pin Configuration and Description(Top view)



Pin No.	Symbol	Description
2, 3	RF IN /VGS	RF Input, Gate Bias
6, 7	RF OUT /VDS	RF Output, Drain Bias
1, 4, 5, 8	NC	No connection
Package Base	GND	DC/RF Ground. Must be soldered to EVB ground plane over array of vias for thermal and RF performance. Solder voids under Pkg Base will result in excessive junction temperatures causing permanent damage.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	125	Vdc
Gate--Source Voltage	V_{GS}	-10,+2	Vdc
Operating Voltage	V_{DD}	40	Vdc
Maximum Forward Gate Current @ T_C = 25°C	Igmax	2.5	mA
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature(See note 1)	T_J	+200	°C
Total Device Power Dissipation (Derated above 25°C, see note 2)	Pdiss	21	W

Note: 1. Continuous operation at maximum junction temperature will affect MTTF
2.Bias Conditions should also satisfy the following expression: Pdiss < (Tj – Tc) / RJC and Tc = Tcase

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, RF CW operation	$R_{\theta JC}$	5.5	℃/W

Table 3. Electrical Characteristics (T_C = 25℃ unless otherwise noted)

DC Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V_{GS}=-8V; I_{DS}=2.5mA	V_{DSS}		125		V
Gate Threshold Voltage	V_{DS} = 28V, I_D =2.5mA	V_{GS}(th)		-2.7		V
Gate Quiescent Voltage	V_{DS} =28V, I_{DS}=30mA, Measured in Functional Test	$V_{GS(Q)}$		-2.46		V

5.1-5.9GHz

TYPICAL CHARACTERISTICS

Figure 2. Power Gain and Drain Efficiency as Function of Pulse Output Power

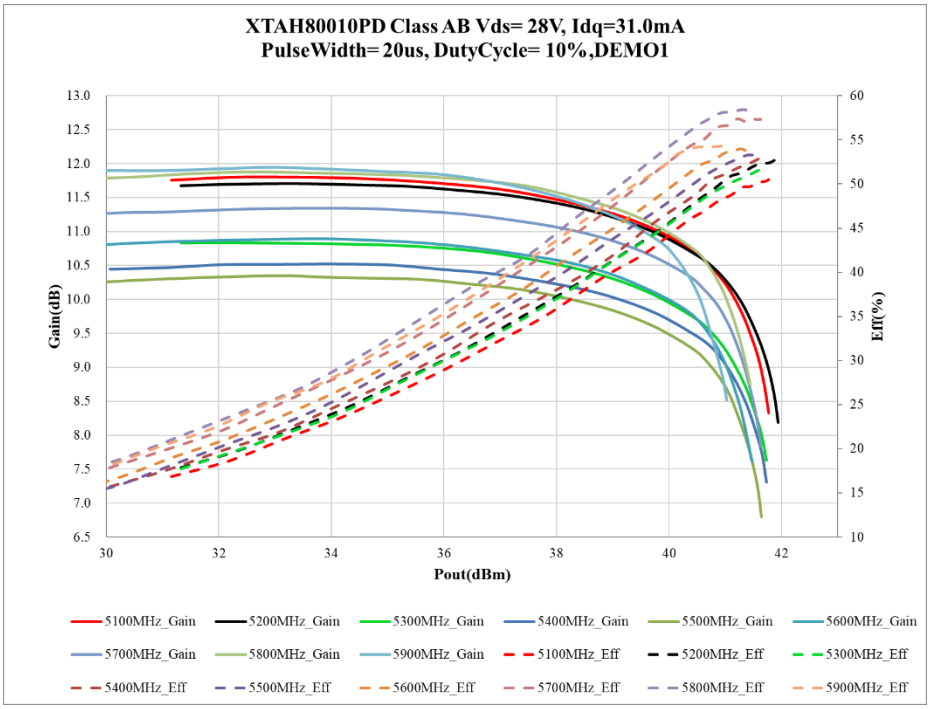
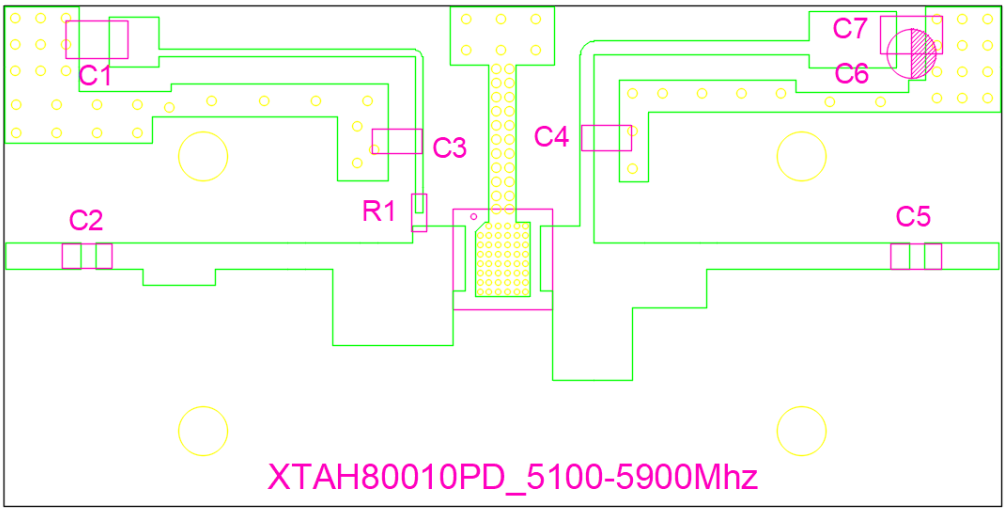


Figure 3. PCB layout and bill of materials



Reference	Footprint	Value	Quantity
C1, C6	1210	10uF/100V	2
C2,C3,C4,C5	0603	3.9pF	4
R1	0603	10Ω	1
C7		470uf/63V	1
U1	DFN4*4	XTAH80010PD	1

7.2-7.8GHz

TYPICAL CHARACTERISTICS

Figure 4. Power Gain and Drain Efficiency as Function of Pulse Output Power

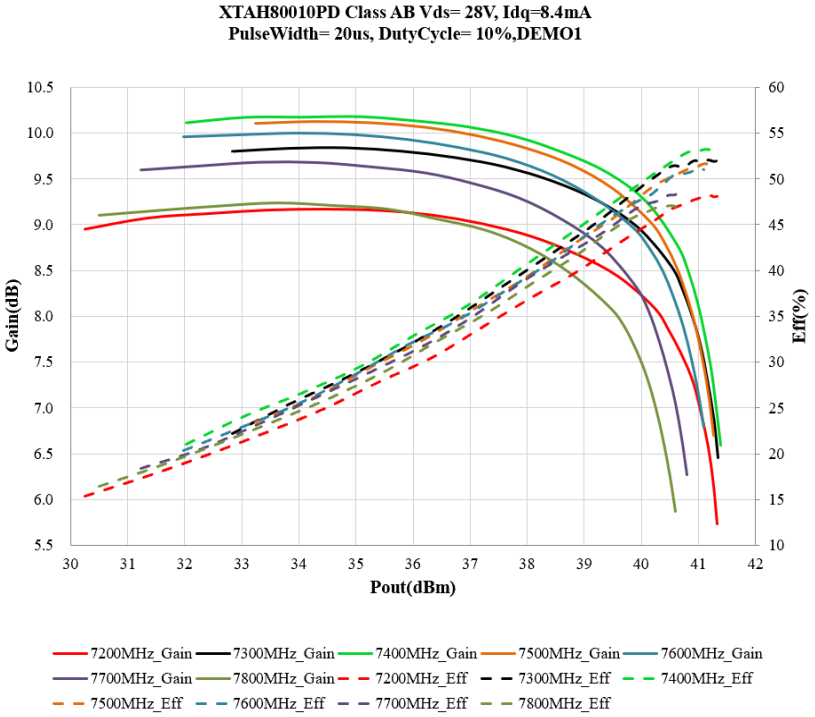
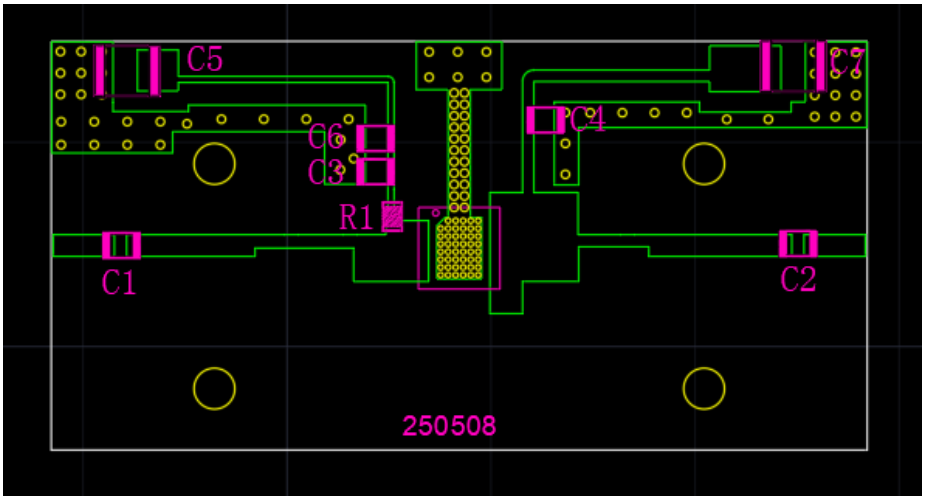


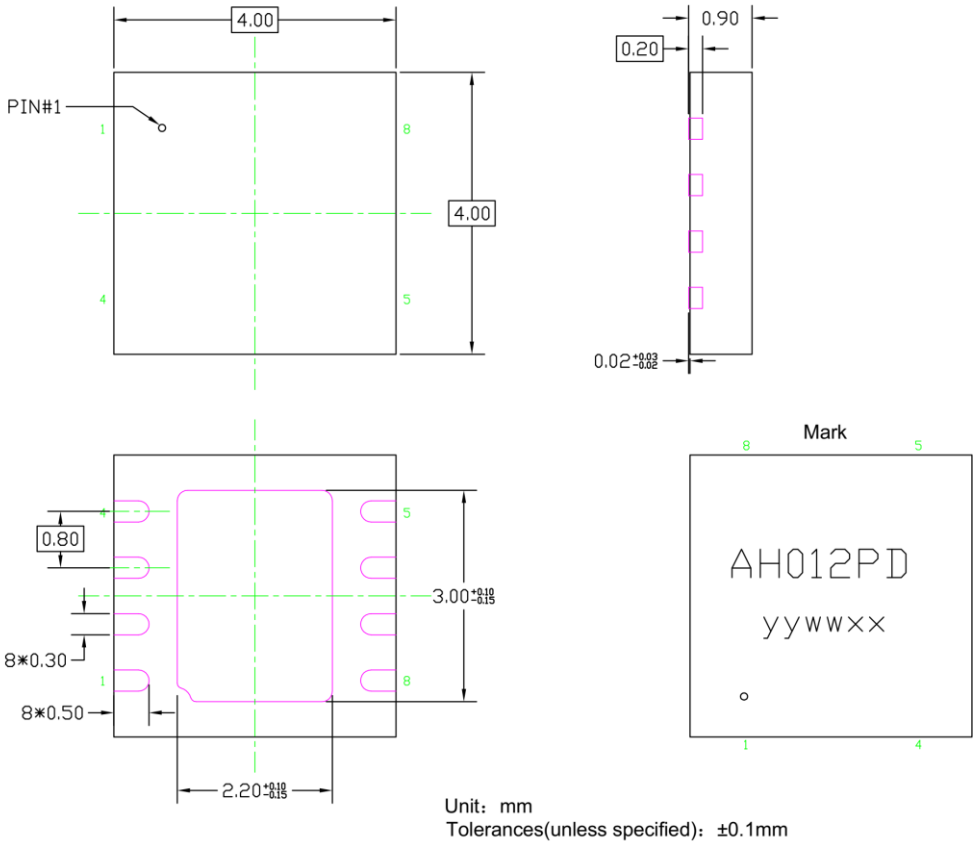
Figure 5. PCB layout and bill of materials



Component	Value	Quantity
U1	XTAH80010PD	1
C1、 C2、C3、 C4	1.8pF	4
C6	10nF/16V	1
C5、 C7	10uF/63V	2
R1	10Ω	1

Package Dimensions

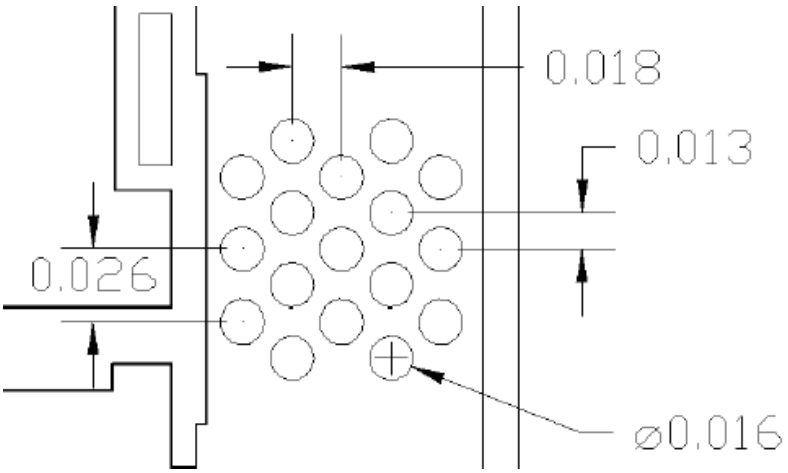
4*4 DFN Package



Notes:

1. All dimensions are in mm;
2. The tolerances unless specified are ±0.1mm.

Recommended vias layout: (all in inches)



Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2025/8/5	**V1.0**	**Preliminary Datasheet Creation**

Application data based on LBG-25-30，ZYX-25-27，CWZ-25-11

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