MF141K2VP LDMOS TRANSISTOR

Document Number: MF141K2VP
Preliminary Datasheet V1.0

1200W, 50V L band RF LDMOS FETs

MF141K2VP

Description

The MF141K2VP is a 1200W, high performance, internally matched LDMOS FET, designed for L band pulsed applications with frequencies 1.2-1.4GHz.It is featured for high power and high ruggedness.

It is recommended to use this device under pulse condition only

- Typical Pulse Performance (on innogration wide band test fixture with device soldered):
  Vds = 50 V, Idq = 100 mA, TA = 25 °C, Pulse condition: 10%, 20us

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
1200	59.95	988.4	57.2	15.68	60.55	1135.1	56.4
1250	60.12	1027.8	54.7	15.49	60.96	1248.8	55.5
1300	60.58	1142.4	53.9	14.28	61.39	1378.5	54.9
1350	60.64	1158.2	53.2	13.69	61.34	1360.5	53.5
1400	59.84	964.9	52.5	14.66	60.6	1147.1	52.7

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Excellent thermal stability, low HCI drift
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	115	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case,Case Temperature 80°C,1300W Pout, Pulse width: 100us, duty cycle: 10%, Vds=50 V, I_{DQ} = 100 mA	$R_{\theta JC}$	0.018	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 °C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit

DC Characteristics

Drain-Source Breakdown Voltage (V_{GS}=0V; I_D=100uA)	V_{DSS}	115			V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50 V, V_{GS} = 0 V)	I_{DSS}			10	μA
Gate--Source Leakage Current (V_{GS} = 6 V, V_{DS} = 0 V)	I_{GSS}			1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600 uA)	$V_{GS(th)}$		1.6		V
Gate Quiescent Voltage (V_{DD} = 50 V, I_{DQ} = 3500 mA, Measured in Functional Test)	$V_{GS(Q)}$		3.8		V

Reference Circuit of Test Fixture

(Layout file upon request) PCB: Roger 4350B, 20mils

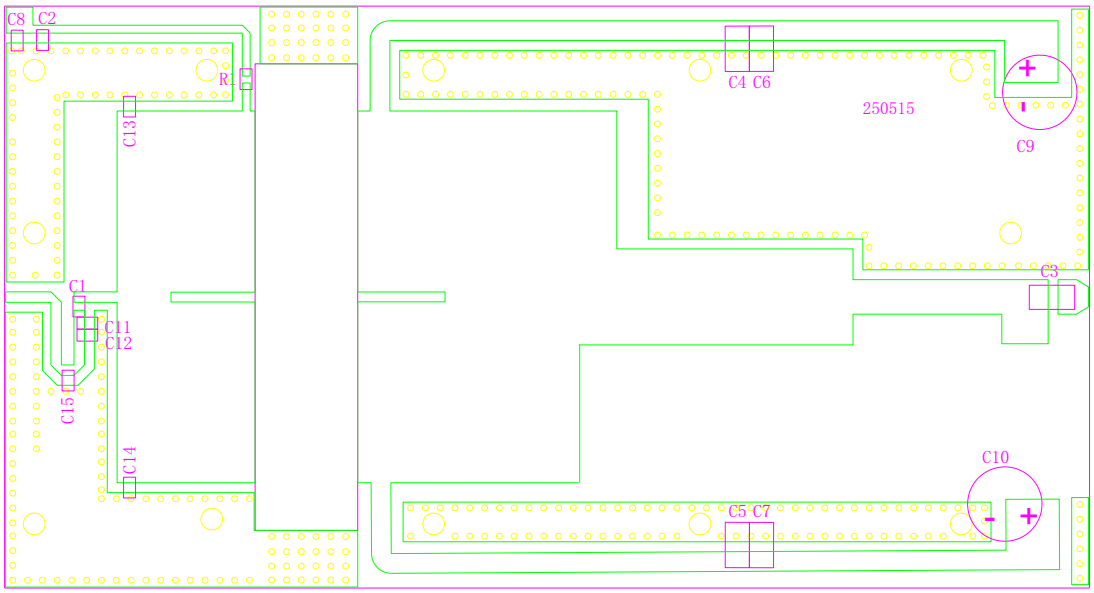


Figure 1. Test Circuit Component Layout

Designator	Comment	Footprint	Quantity
C1	10 pF	0603/0805	1
C2	47 pF	0603/0805	1
C3, C4, C5,	47 pF	1210	3
C6, C7	10uF/100V	1210	2
C8	10uF/16V	0603/0805	1
C9, C10	1000uF/63V		2
C11, C12, C13, C14	3.0pF	0603/0805	1
C15	1.5 pF	0603/0805	3
R1	10 Ω	0603/0805	1

TYPICAL CHARACTERISTICS

Figure 2: Power gain and Efficiency as a Function of Pout

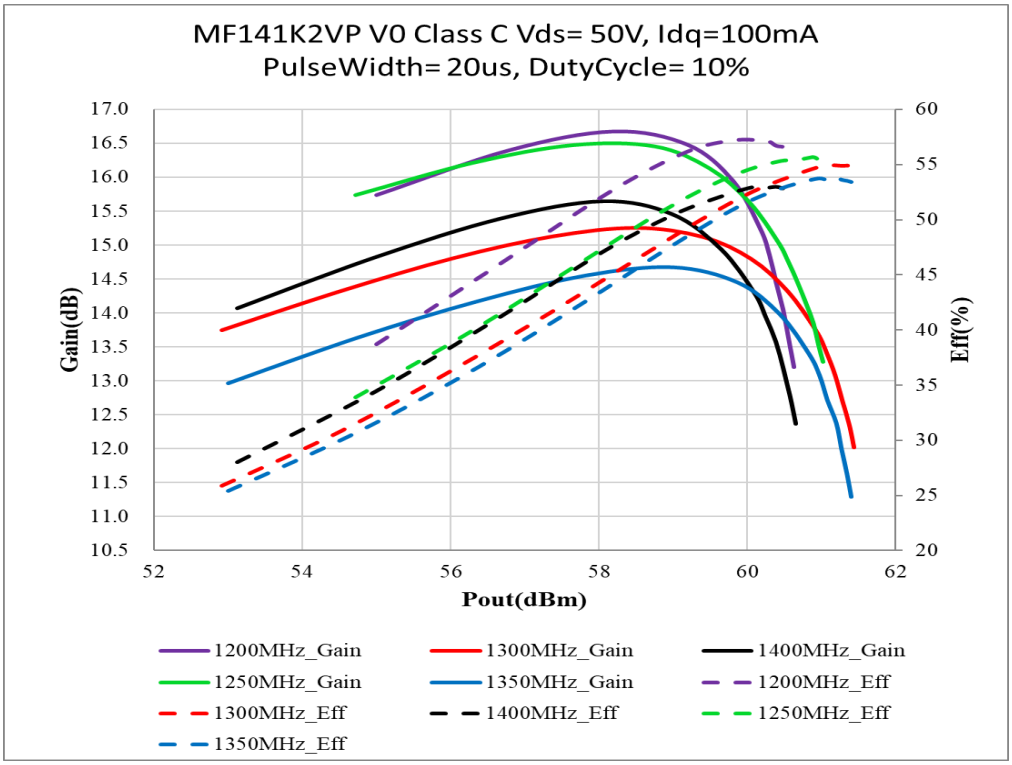
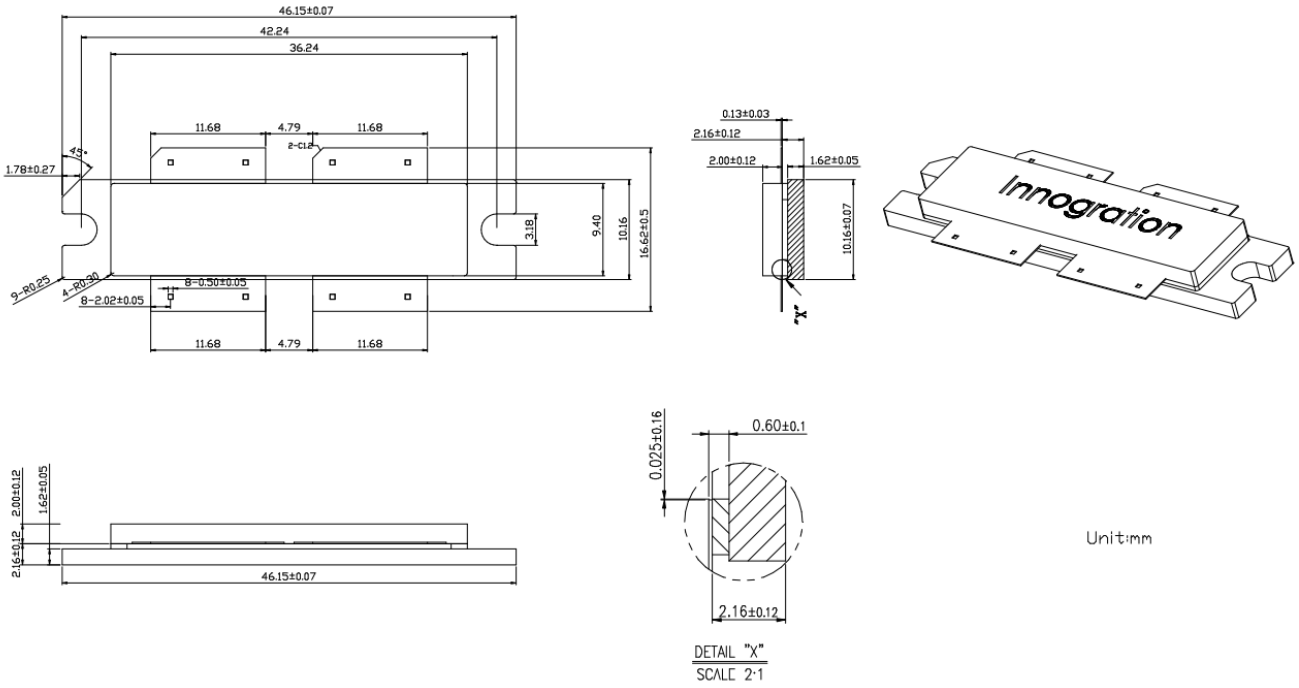


Figure 3: Network analyzer S11 and S21

Package Outline

Flanged ceramic package;



OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-O4E					5/6/2024

Revision history

Table 6. Document revision history

Date	Revision	Datasheet Status
2025/8/11	Rev 1.0	Preliminary Datasheet Creation

Application data based on LSM-25-23

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