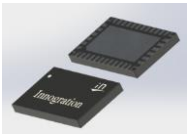
10W,12V Matched RF LDMOS Amplifier

IMEN1415-10



Description

The IMEN1415-10 is a 10-watt, highly rugged, input fully matched and output partially matched LDMOS FET, designed for multiple applications within 1.4-1.5GHz It can be used in linear or saturated power amplifier, for CW and pulsed signal, and any modulation format in highly compact PCB.

It is also featured by its lower cost of plastic open cavity for surface mount on PCB through vias

- Typical Performance **in compact PCB** (On Innogration fixture with device soldered).

VDS= 12V, Vpeak=-2.80V, IDQ=200mA CW and pulse					
Freq (MHz)	**P-1(dBm)**	**P-1Gain（dB）**	**P-3(dBm)**	**P-3(W)**	**EFF (%)**
1300	39.61	12.79	40.59	11.5	39.6
1350	38.57	13.64	40.17	10.4	39.6
1400	**39.26**	**15.1**	**41.25**	**13.4**	**50.3**
1450	**38.39**	**15.9**	**40.83**	**12.1**	**54.6**
1500	**37.89**	**15.8**	**40.28**	**10.7**	**59.0**
1550	36.38	14.92	38.79	7.6	53.8
1600	35.97	13.72	38.28	6.7	51.5

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- GPS/Beidou power amplifier
- 1.4GHz image transmission

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+40	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+13.6	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	$R_{\theta JC}$	2	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage V_{GS}=0, I_{DS}=100uA	$V_{(BR)DSS}$		70		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 12.5V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate--Source Leakage Current (V_{GS} = 9 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 12.5V, I_D = 600 μA)	$V_{GS}(th)$	——	2	——	V
Gate Quiescent Voltage (V_{DD} = 12.5V, I_D = 100mA, Measured in Functional Test)	$V_{GS(Q)}$	——	3.3	——	V

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 12.5Vdc, I_{DQ} = 100 mA, f = 1000 MHz

VSWR 10:1 at 10W pulse CW Output Power	No Device Degradation

Figure 1:Pin Definition(Top View)

Pin No.	Symbol	Description
2,5,7,12,13,18,20,23,25,30,31,36	GND	DC/RF Ground
1	Vgs	
6	RF in	
21,22	Vds/RF out	
Others	NC	Not connected
Package Base	GND	DC/RF Ground.

Reference Circuit of Test Fixture Assembly Diagram

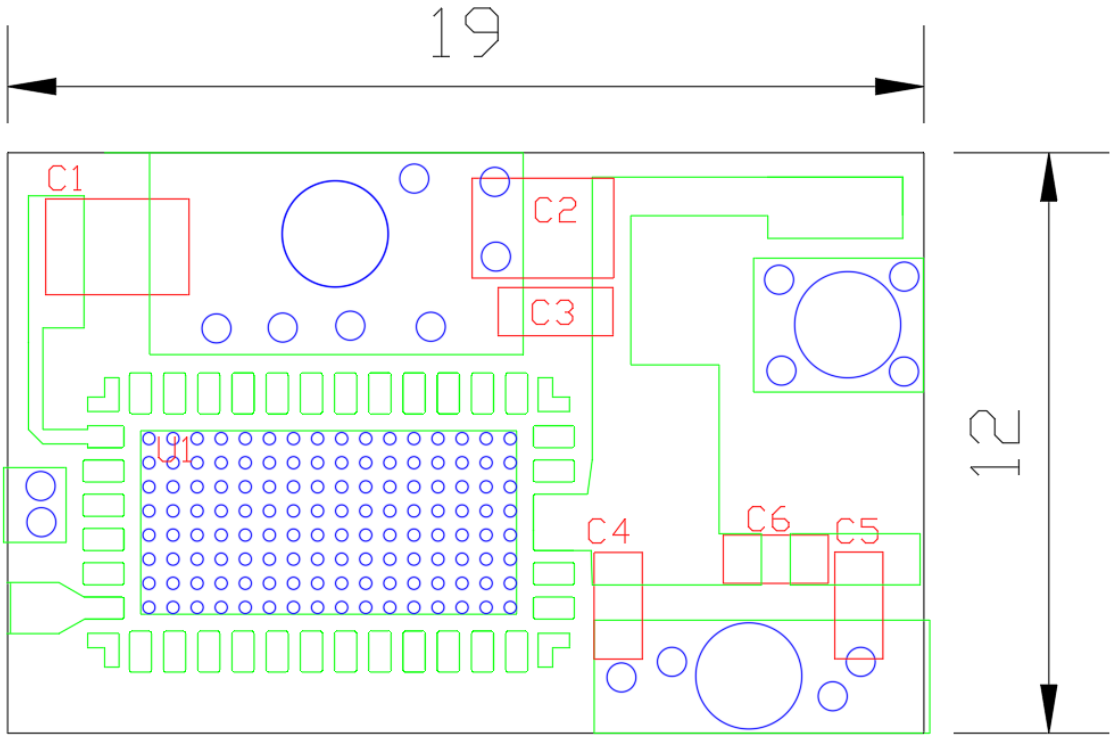


Figure 2. Test Circuit Component Layout

Table 5. Test Circuit Component Designations and Values

Component	Value	Footprint
U1	IMEN1415-10	10.0*6.0mm
C1,C2	10uf	1020
C3,C6	30pF	0603
C4,C5	3.9pF	0603

Typical performance

Figure 3： Power gain efficiency as function of Pout

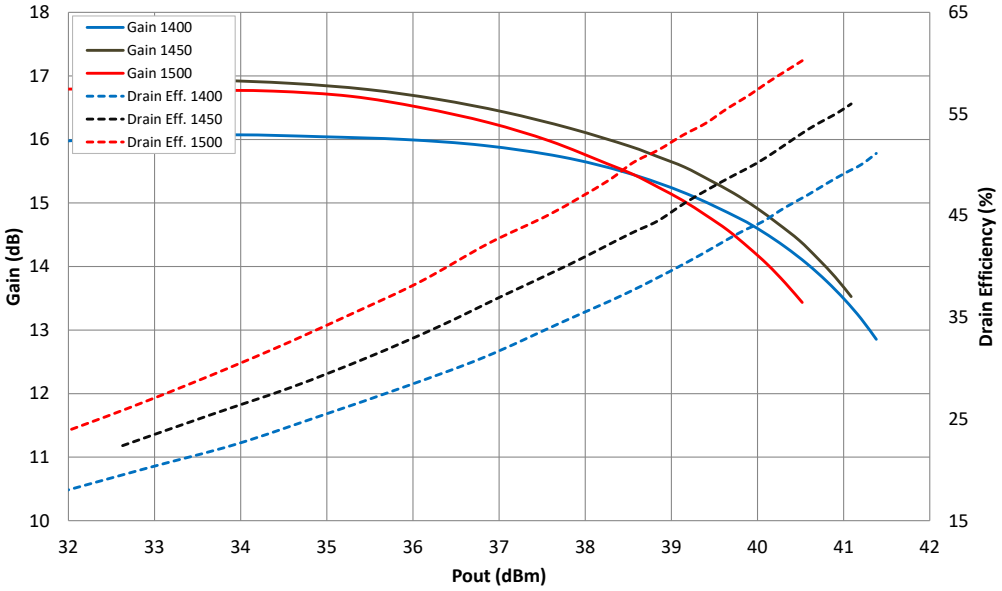
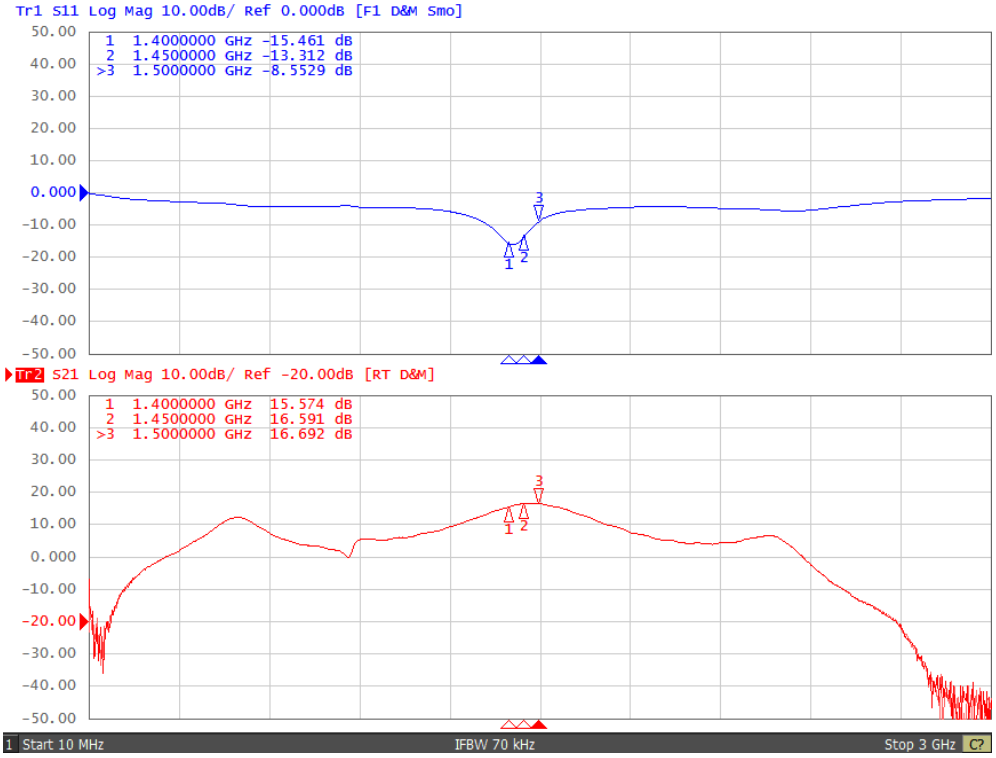
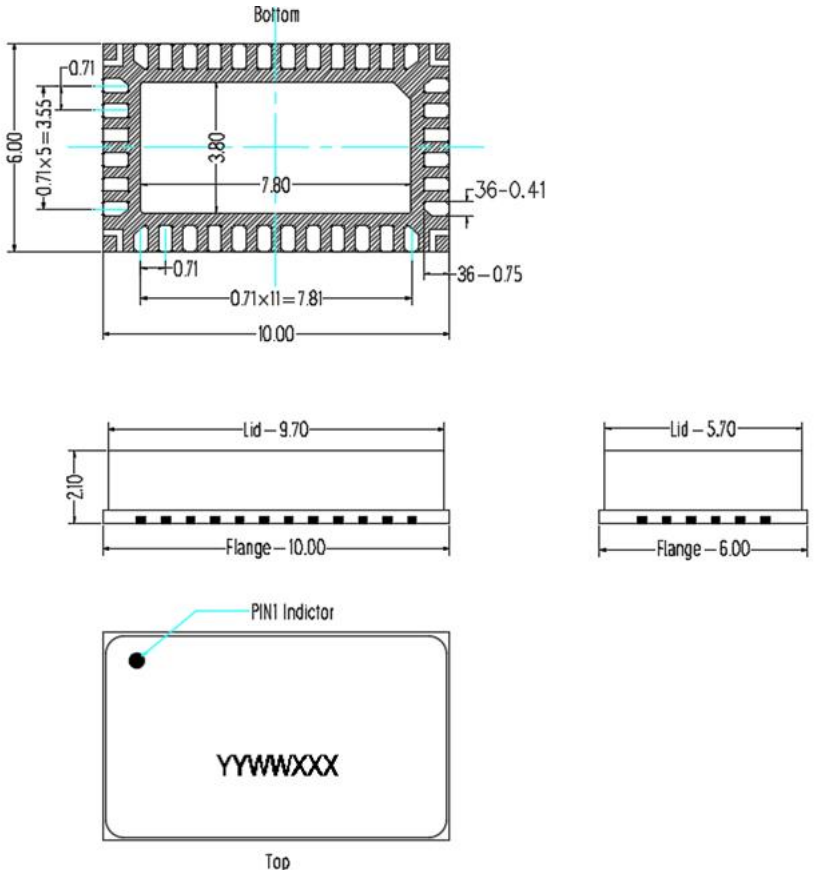


Figure 4： Network analyzer out Pout S11/S21



Package Dimensions

10*6 Plastic Package



Notes:

1. All dimensions are in mm;
2. The tolerances unless specified are ±0.2mm.

Revision history

Table 7. Document revision history

Date	Revision	Datasheet Status
2025/8/22	Rev 1.0	Preliminary Datasheet as replacement of ITEH09070C6

Application data based on HJ-25-11

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