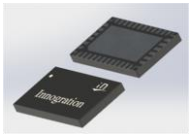
GaN 28V, 40W, HF to L band RF Power Transistor

STBH20040C6



Description

The STBH20040C6 is a 40W GaN HEMT, designed for multiple applications, up to 2GHz.

The transistor is available in a highly cost effective 10*6mm, surface mount, QFN package with 100% DC production test to ensure the quality and consistency.

It can be used in CW, Pulse and any other modulation modes.

There is no guarantee of performance when this part is used in applications designed Outside of these frequencies.

- Typical1.1-1.7G CW RF Performance with device soldered through high density and plated grounding vias
  Vds = 28V, Idq = 25mA,Vgs=-2.37V

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
1100	45.30	33.92	65.57	15.97	46.35	43.10	73.29
1200	45.33	34.15	68.99	16.48	46.33	42.91	76.64
1300	45.40	34.69	70.58	17.49	46.38	43.46	77.34
1400	45.43	34.92	70.06	17.23	46.52	46.52	78.14
1500	45.37	34.47	66.10	16.67	46.57	45.40	73.29
1600	45.13	32.60	62.88	16.74	46.57	45.42	70.98
1700	44.72	29.67	64.38	16.65	46.16	41.31	72.57

Applications

- HF to UHF band power amplifier
- L band power amplifier
- ISM/RF Energy power amplifier

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

Turning the device ON

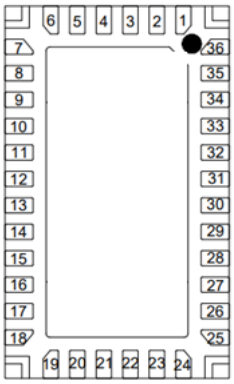
1. Set VGS to the pinch--off (VP) voltage, typically –5 V
2. Turn on VDS to nominal supply voltage
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically –5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

Figure 1: Pin Connection definition

Transparent top view (Backside grounding for source)



Pin No.	Symbol	Description
8,9,10,11,14,15,16,17	RF IN/Vgs	RF Input, Vgs bias

26,27,28,29,32,33,34,35	RF OUT/VDD	RFOutput, Drain bias
Rest Pins and Package Base	GND	DC/RF Ground. Must be soldered directly to heatsink or copper coin for CW application.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+200	Vdc
Gate--Source Voltage	V_{GS}	-8 to +0.5	Vdc
Operating Voltage	V_{DD}	36	Vdc
Maximum gate current	Igs	10	mA
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case by FEA T_C= 85°C, at Pdiss=20W	$R_{\theta JC}$	4	°C /W

Table 3. Electrical Characteristics (TA = 25℃ unless otherwise noted)

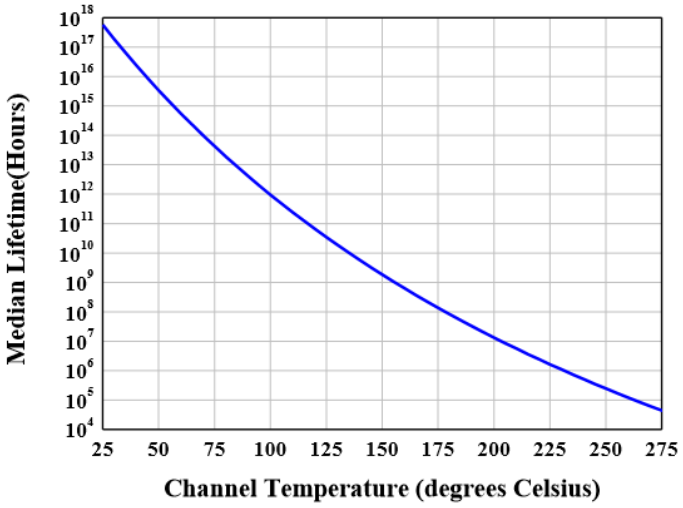
DC Characteristics (main path, measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	VGS=-8V; IDS=10mA	V_{DSS}		200		V
Gate Threshold Voltage	VDS =10V, ID = 10mA	$V_{GS(th)}$	-4		-2	V
Gate Quiescent Voltage	VDS =28V, IDS=100mA, Measured in Functional Test	$V_{GS(Q)}$		-3.3		V

Ruggedness Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Load mismatch capability	1.6GHz, Pout=40W Pulsed CW All phase, No device damages	VSWR		10:1		

Figure 2: Median Lifetime vs. Channel Temperature



1.1-1.7GHz

Typical performance

Figure 3: Efficiency and power gain as function of Pout

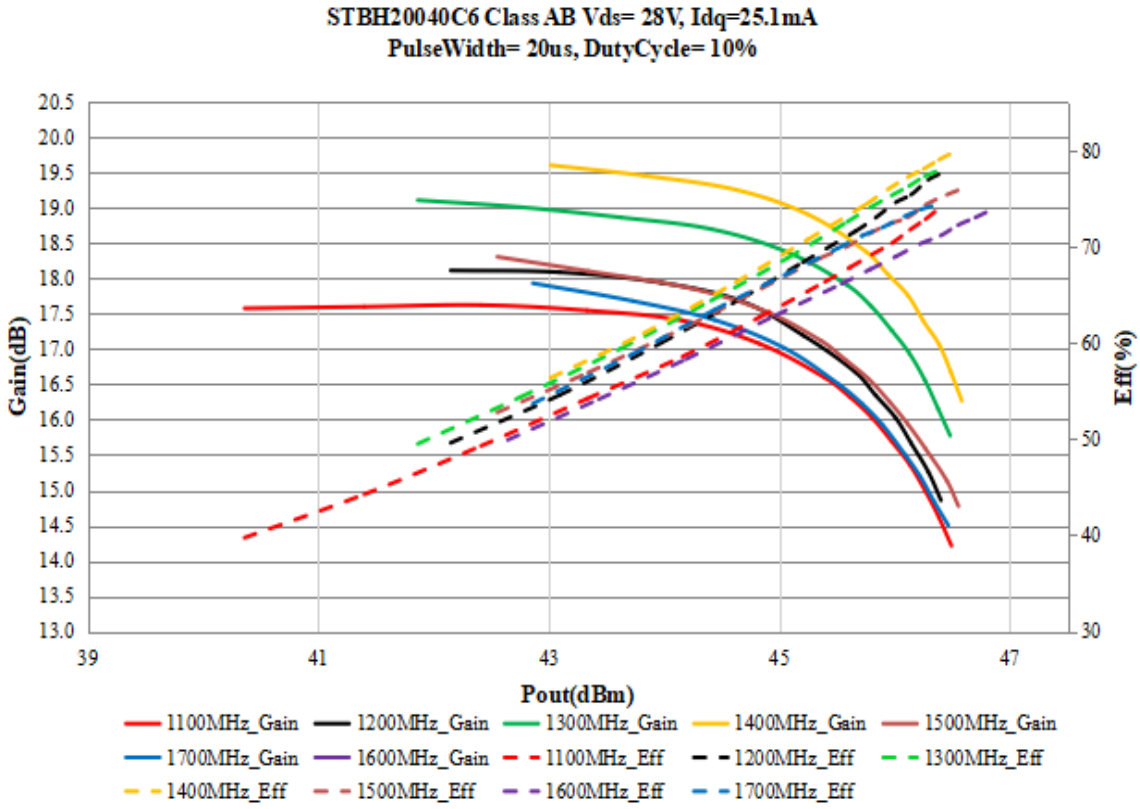


Figure 4: Network analyzer output S11/S21

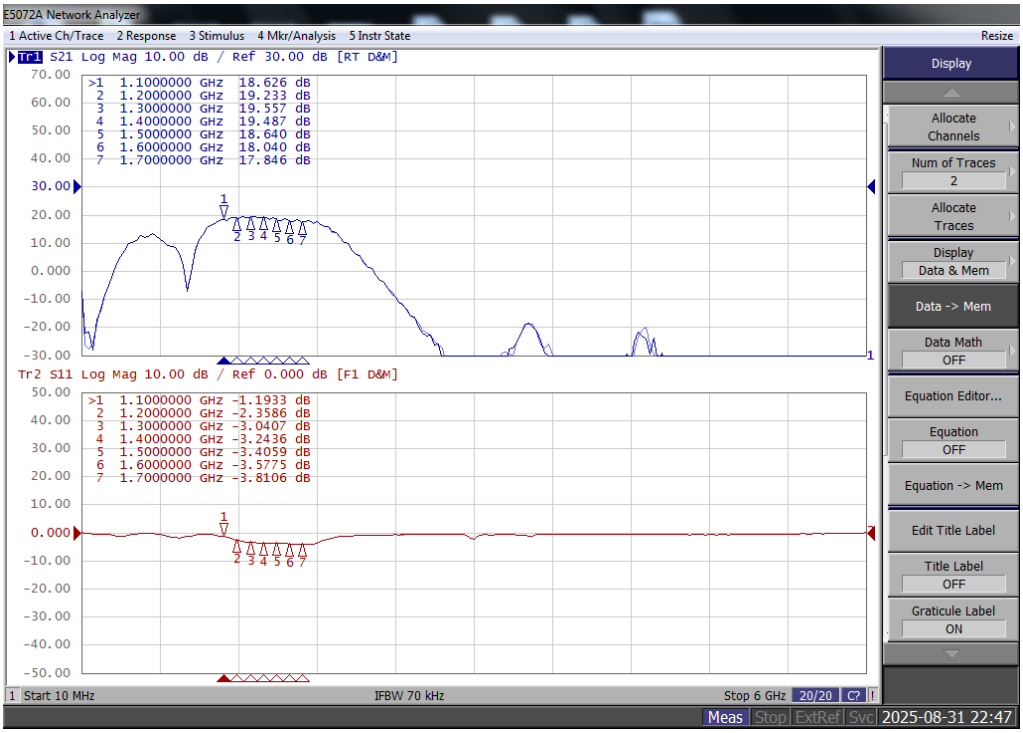


Figure 5: Picture of application board

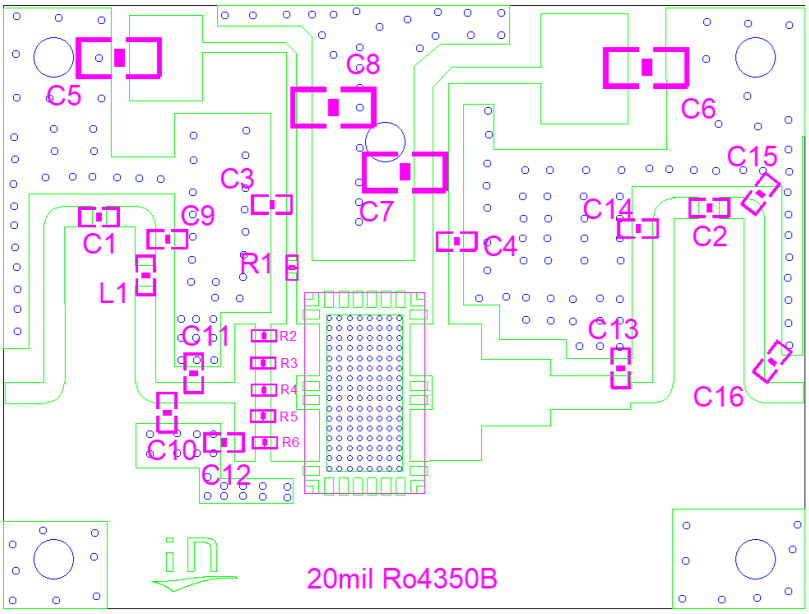
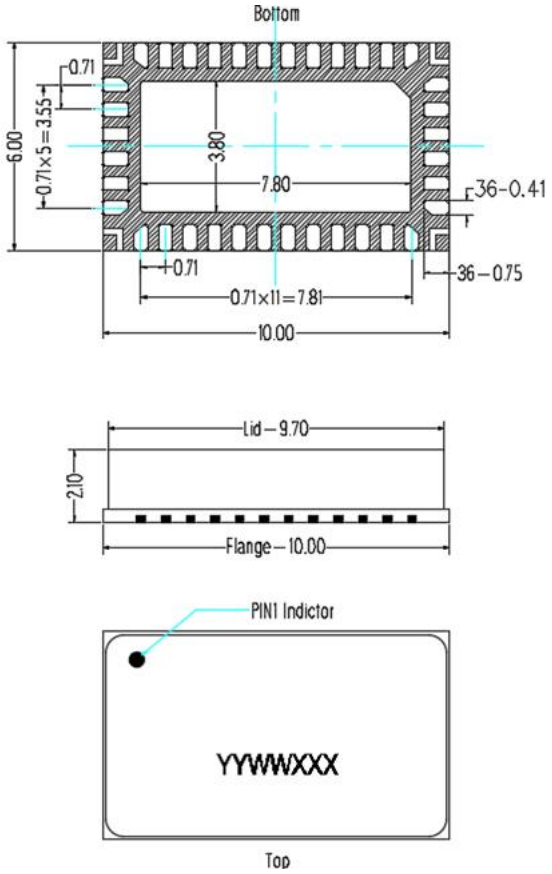


Table 4. Bill of materials of application board (PCB layout upon request, RO4350B 20mils)

C1	1	3.9pFHigh Q Capacitor	251SHS3R9BSE	TEMEX
C2,C3,C4	3	30pFHigh Q Capacitor	251SHS30BSE	TEMEX
C9	1	1.0pFHigh Q Capacitor	251SHS1R0BSE	TEMEX
C10	1	3pFHigh Q Capacitor	251SHS3R0BSE	TEMEX
C11	1	5.1pFHigh Q Capacitor	251SHS5R1BSE	TEMEX
C12	1	1.8pFHigh Q Capacitor	251SHS1R8BSE	TEMEX
C13	1	3.9pFHigh Q Capacitor	251SHS3R9BSE	TEMEX
C14	1	0.5pFHigh Q Capacitor	251SHS0R5BSE	TEMEX
C15	1	0.2pFHigh Q Capacitor	251SHS0R2BSE	TEMEX
C16	1	0.6pFHigh Q Capacitor	251SHS0R6BSE	TEMEX
C5,C6,C7,C8	4	10uF MLCC	GRM32EC72A106ME05	Murata
L1	1	1.5nH Inductance	/	/
R1	1	10Ω Power Resistor	ESR03EZPF100	ROHM
R2,R3,R4,R5,R6	1	5Ω Power Resistor	ESR03EZPF100	ROHM
T1	1	GaN Transistor	STBH20040C6	Innogration

10*6 Plastic Package



Notes:

1. All dimensions are in mm;
2. The tolerances unless specified are ±0.2mm.

Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2025/9/1	**V1.0**	**Preliminary Datasheet Creation**

Application data based on: HZH-25-08

Notice

Specifications are subject to change without notice. Innogration believes the information within the data sheet to be reliable. Innogration makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose.
"Typical" parameter is the average values expected by Innogration in quantities and are provided for information purposes only. It can and do vary in different applications and related performance can vary over time. All parameters should be validated by customer's technical experts for each application.
Innogration products are not designed, intended or authorized for use as components in applications intended for surgical implant into the body or to support or sustain life, in applications in which the failure of the Innogration product could result in personal injury or death or in applications for planning, construction, maintenance or direct operation of a nuclear facility.
For any concerns or questions related to terms or conditions, please check with Innogration and authorized distributors