

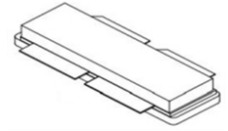


GaN 50V,UHF to L band 600W, RF Power Transistor

SQ1560RVPS

Description

The SQ1560RVPS is a push pull 600W capable, internally matched GaN HEMT, ideal for multiple applications up to 1.5GHz. It is optimized thermally to support higher duty cycle or longer pulse up to CW application. **In typical wideband application from 960 to 1225MHz, it can deliver >450W CW across the full band.**



There is no guarantee of performance when this part is used outside of stated frequencies.

SQ1560RVPS VDD=48V Vgs=-3.43V Idq=150mA,CW							Harmonic	
F (MHz)	Pin (dBm)	Pout (dBm)	Psat (W)	Id (A)	Gain (dB)	Eff (%)	2 nd	3 th
960	45.1	57.23	528	17.84	12.1	61.7	-38.8	-37.6
1000	45.1	57.85	610	18.50	12.8	68.6	-38.6	-33.4
1050	45	57.35	543	16.10	12.4	70.3	-39.1	-37.6
1100	44.9	56.85	484	14.30	12.0	70.5	-42.3	-38.3
1150	44.9	56.65	462	15.86	11.8	60.7	-27.4	-51
1200	44.7	56.66	463	16.60	12.0	58.2	-40.6	-45
1250	45	56.60	457	16.20	11.6	58.8	-39.2	-41.1

Applications

- L/P band power amplifier
- UHF TV
- Public Safety Radio
- Data link power amplifier

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

Turning the device ON

1. Set VGS to the pinch--off (VP) voltage, typically -5 V
2. Turn on VDS to nominal supply voltage
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically -5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V _{DSS}	+200	Vdc
Gate--Source Voltage	V _{GS}	-8 to +0.5	Vdc
Operating Voltage	V _{DD}	55	Vdc
Maximum gate current	I _{gs}	86.6	mA
Storage Temperature Range	T _{stg}	-65 to +150	°C
Case Operating Temperature	T _C	+150	°C
Operating Junction Temperature	T _J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case by FEA	R _{θJC}	0.3	°C /W



T_C= 25°C, at P_{out}=600W @900MHz

Table 3. Electrical Characteristics (TA = 25°C unless otherwise noted)

DC Characteristics (Each path, measured on wafer prior to packaging)

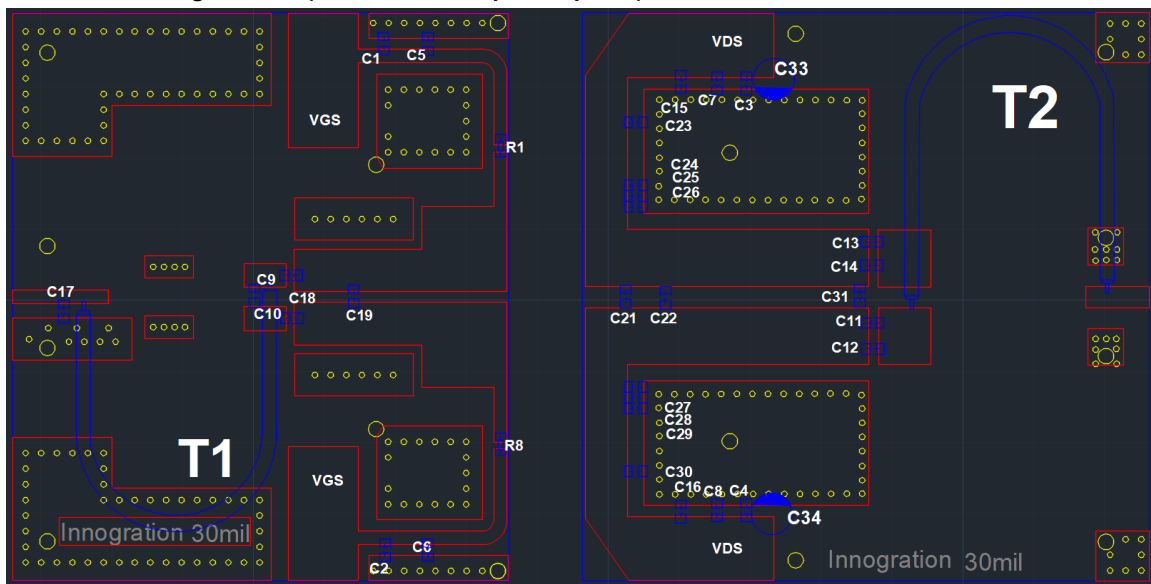
Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V _{GS} =-8V; I _{DS} =36mA	V _{DSS}		200		V
Gate Threshold Voltage	V _{DS} =10V, I _D = 36mA	V _{GS(th)}	-4	-	-2	V
Gate Quiescent Voltage	V _{DS} =50V, I _{DS} =800mA, Measured in Functional Test	V _{GS(Q)}		-3.3		V

Ruggedness Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Load mismatch capability	900MHz, P _{out} =600W pulse CW All phase, No device damages	VSWR		5:1		

960-1225MHz

Figure 1: Reference design circuit (PCB DWG file upon request,)



Component	Description	Suggested Manufacturer
C1,C2,C3,C4	10uF	10uF/100V
C5,C6	39pF	
C7,C8	100pF	
C9,C10	56pF	
C11,C12,C13,C14	20pF	
C15,C16	91pF	
C17,C19	2pF	
C18	1.2pF	
C20	6.2pF	
C21	4.7pF	



C22,C27,C28,C29,C30	2.4pF	
C23	1pF	
C24,C25,C26	0.8pF	
C31,C32	0.5pF	
C33,C34	4700uF/50V	Electrolytic Capacitor
R1,R8	10 Ω	Chip Resistor
T1	25 ohm,50mm	RFSFBU-086-25
T2	35 ohm ,80mm	SFF-35-3
PCB	30Mil Rogers4350b	

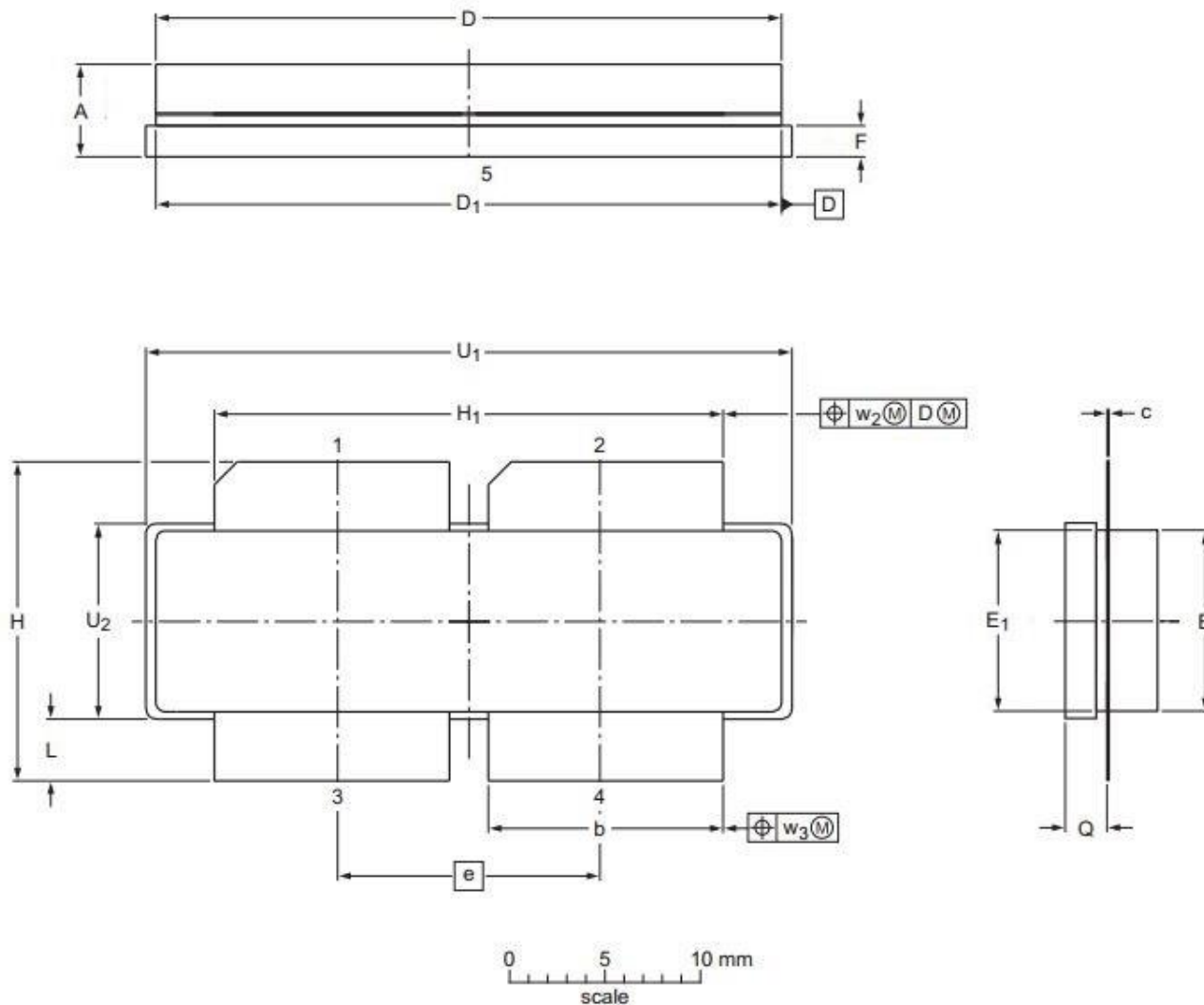
Figure 2: Network analyzer output S21/S11 (Vds=50V, Idq=600mA)





Package Outline

Earless flanged ceramic package; 4 leads (1、2—DRAIN、3、4—GATE、5—SOURCE)



UNIT	A	b	c	D	D ₁	e	E	E ₁	F	H	H ₁	L	Q	U ₁	U ₂	W ₂	W ₂
mm	4.7	11.81	0.18	31.55	31.52	13.72	9.50	9.53	1.75	17.12	25.53	3.48	2.26	32.39	10.29	0.25	0.25
	4.2	11.56	0.10	30.94	30.96		9.30	9.27	1.50	16.10	25.27	2.97	2.01	32.13	10.03		
inches	0.185	0.465	0.007	1.242	1.241	0.540	0.374	0.375	0.069	0.674	1.005	0.137	0.089	1.275	0.405	0.01	0.01
	0.165	0.455	0.004	1.218	1.219		0.366	0.365	0.059	0.634	0.995	0.117	0.079	1.265	0.395		

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-D4					03/12/2013



Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2025/9/8	V1.0	Preliminary Datasheet Creation

Application data based on:SYX-25-32

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