

S3K1665V GaN TRANSISTOR

Document Number: S3K1665V
Preliminary Datasheet V1.0

GaN 50V, 650W, L band RF Power Transistor

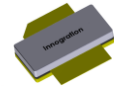
Description

The S3K1665V is a 650-watt, internally matched GaN HEMT, designed for pulsed amplifier applications with frequencies from 1.2-1.6GHz.

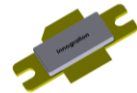
There is no guarantee of performance when this part is used in applications designed outside of these frequencies.

It is recommended to use this device only at pulse condition, and power rating might vary according to different pulse width and duty cycle

S3K1665VS



S3K1665V



- Typical **pulse** Performance (On Innogration **1.2-1.6GHz** fixture with device soldered):

$V_{DD} = 50$ Volts, $I_{DQ} = 100$ mA, Pulse CW, Pulse width=50us, Duty cycle=10%.

Freq (MHz)	Pin (dBm)	Id (A)	Pout (dBm)	Pout (W)	Gain (dB)	Eff (%)
1200	43.5	2.39	58.74	747.4	15.24	65.79
1250	43.5	2.37	58.38	689.0	14.88	61.25
1300	43.5	2.41	58.21	661.9	14.71	58.05
1350	43.5	2.46	58.26	669.4	14.76	57.26
1400	43.5	2.57	58.62	727.3	15.12	60.01
1450	43.5	2.62	58.41	692.8	14.91	56.40
1500	43.5	2.74	58.81	761.2	15.31	59.00
1550	43.5	2.73	58.97	788.4	15.47	61.20
1600	43.5	2.61	58.83	764.4	15.33	62.14

Applications and Features

- Suitable for broad band application in L band
- Thermally Enhanced Industry Standard Package
- High Reliability Metallization Process
- Excellent thermal Stability and Excellent Ruggedness
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

■ Turning the device ON

- 1) Set VGS to the pinch-off (VP) voltage, typically -5 V
- 2) Turn on VDS to nominal supply voltage (50 V)
- 3) Increase VGS until IDS current is attained
- 4) Apply RF input power to desired level

■ Turning the device OFF

- 1) Turn RF power off
- 2) Reduce VGS down to VP, typically -5 V
- 3) Reduce VDS down to 0 V
- 4) Turn off VGS

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DS}	+200	Vdc

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Gate--Source Voltage	V_{GS}	-8 to +0	Vdc
Operating Voltage	V_{DD}	0 to 55	Vdc
Maximum Forward Gate Current @ $T_C = 25^{\circ}C$	I_{gmax}	108	mA
Storage Temperature Range	T_{stg}	-65 to +150	$^{\circ}C$
Case Operating Temperature	T_C	+150	$^{\circ}C$
Operating Junction Temperature	T_J	+225	$^{\circ}C$

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case, $P_{OUT}=650W$ 1.4GHz 20us/10%, $T_{case}=85^{\circ}C$, 50 Vdc, $I_{DQ}=100$ mA	$R_{\theta JC}$	0.3	$^{\circ}C/W$

Table 3. Electrical Characteristics ($T_A = 25^{\circ}C$ unless otherwise noted)

DC Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS}=-8V$; $I_{DS}=108mA$	V_{DSS}	---	200	---	V
Gate Threshold Voltage	$V_{DS} = 10V$, $I_D = 108mA$	$V_{GS(th)}$	-4		-2	V
Gate Quiescent Voltage	$V_{DS} = 50V$, $I_{DS}=1000mA$, Measured in Functional Test	$V_{GS(Q)}$	---	-2.97	---	V

Load Mismatch (In Innogration Test Fixture, 50 ohm system): $V_{DD} = 50$ Vdc, $I_{DQ} = 100$ mA, $f = 1400$ MHz

VSWR 10:1 at 650W pulse CW Output Power	No Device Degradation
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TYPICAL CHARACTERISTICS

1.2-1.6GHz

Figure 1. Power Gain and Drain Efficiency as Function of Pulse Output Power

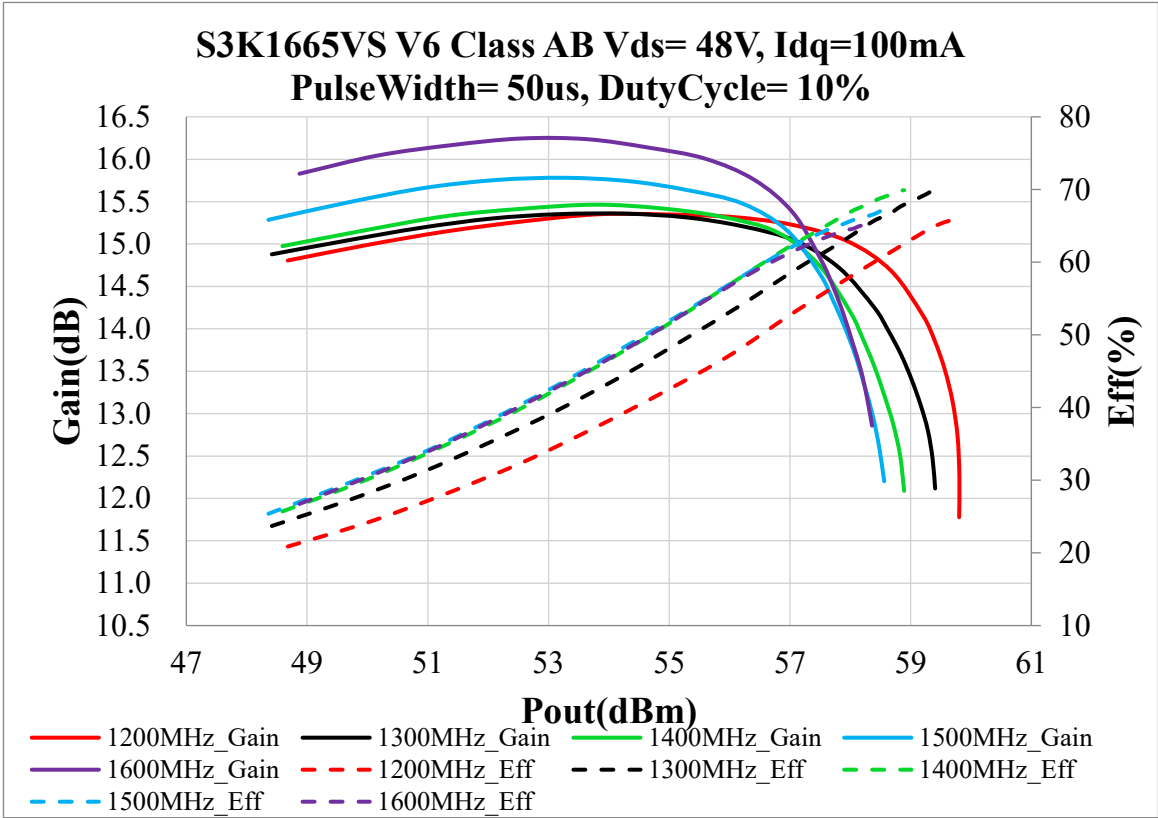


Figure 2. Network analyzer output S11/S21

$V_{DS}=50V$ $I_{DQ}=1000mA$ $V_{GS}=-3V$

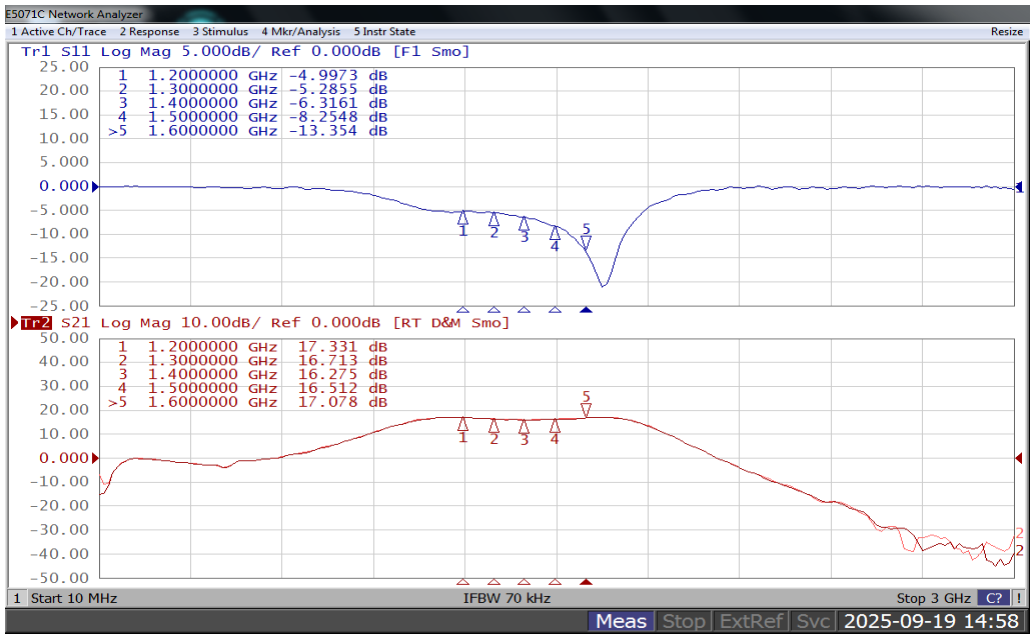


Figure 3. Test Circuit Component Layout

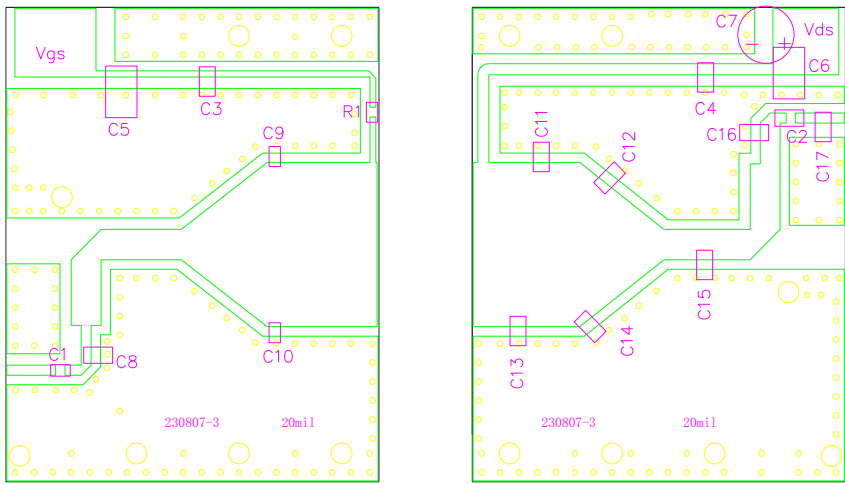


Table 4. Test Circuit Component Designations and Values

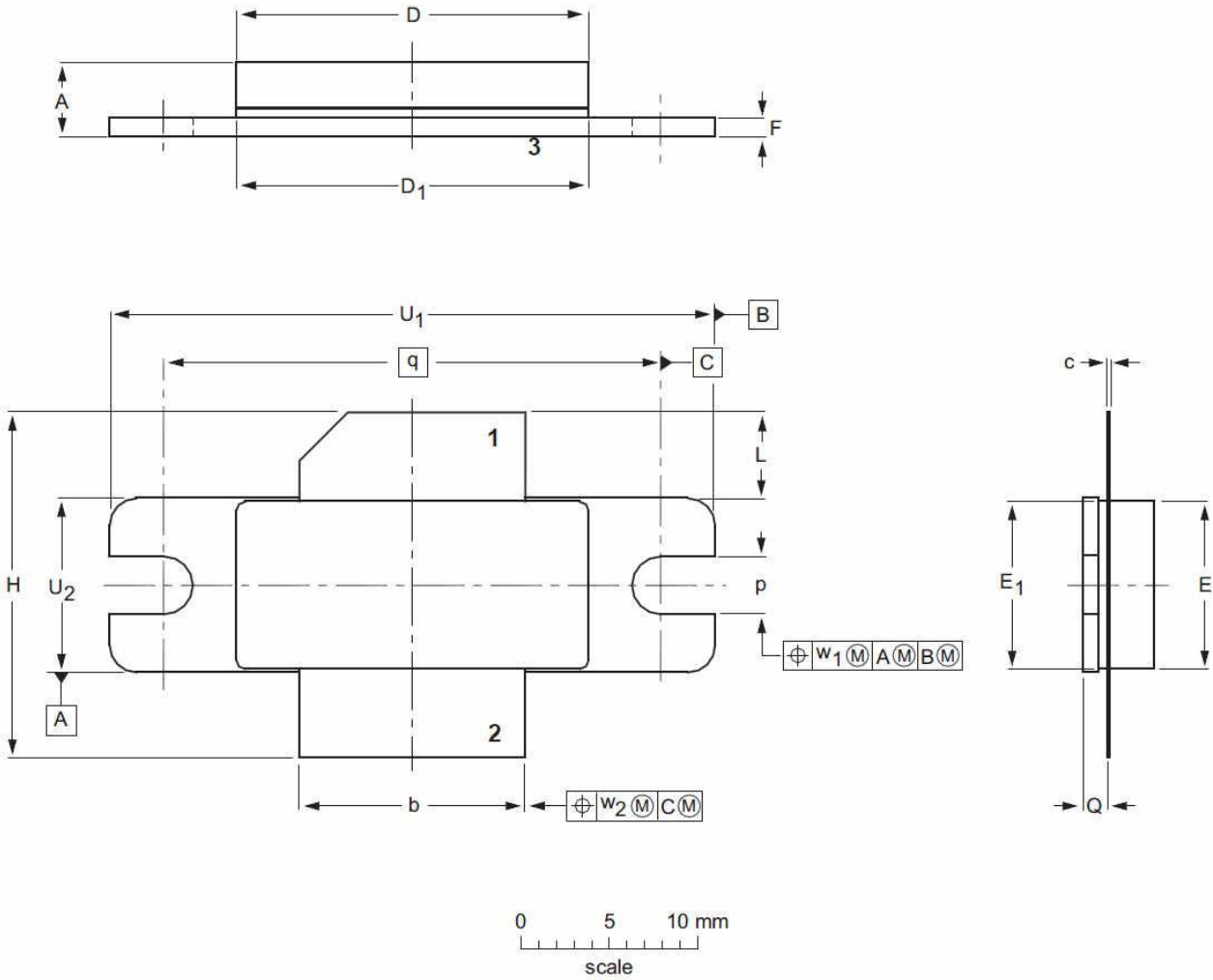
Designator	Comment	Footprint	Quantity
C1	4.7 pF	0805	1
C2, C3, C4,	47 pF	0805	3
C5, C6	10uF/100V	1210	2
C7	1000uF/63V		1
C8, C17	0.2 pF	0805	2
C9, C10	3.3pF	0805	2
C11, C12, C13, C14, C15	3.0pF	0805	5
C16	0.8 pF	0805	1
R1	10 Ω	0603	1

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Package Outline

Flanged ceramic package; 2 mounting holes; 2 leads (1—DRAIN、2—GATE、3—SOURCE)



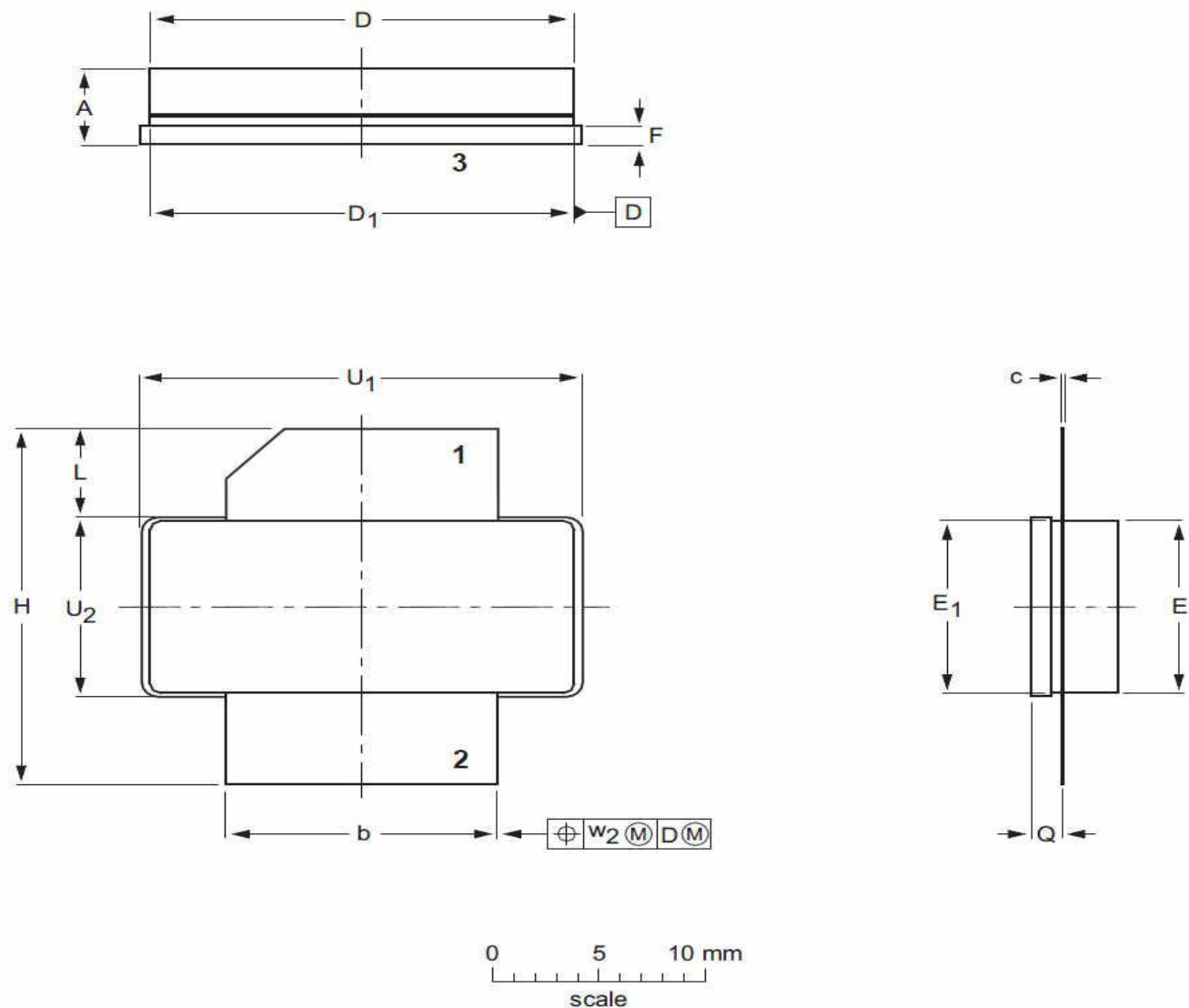
UNIT	A	b	c	D	D ₁	E	E ₁	F	H	L	p	Q	q	U ₁	U ₂	W ₁	W ₂
mm	4.72	12.83	0.15	20.02	19.96	9.50	9.53	1.14	19.94	5.33	3.38	1.70	27.94	34.16	9.91	0.25	0.51
	3.43	12.57	0.08	19.61	19.66	9.30	9.25	0.89	18.92	4.32	3.12	1.45		33.91	9.65		
inches	0.186	0.505	0.006	0.788	0.786	0.374	0.375	0.045	0.785	0.210	0.133	0.067	1.100	1.345	0.390	0.01	0.02
	0.135	0.495	0.003	0.772	0.774	0.366	0.364	0.035	0.745	0.170	0.123	0.057		1.335	0.380		

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B2E					03/12/2013

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Earless flanged ceramic package; 2 leads (1—DRAIN、2—GATE、3—SOURCE)



UNIT	A	b	c	D	D ₁	E	E ₁	F	H	L	Q	U ₁	U ₂	W ₂
mm	4.72	12.83	0.15	20.02	19.96	9.50	9.53	1.14	19.94	5.33	1.70	20.70	9.91	0.25
	3.43	12.57	0.08	19.61	19.66	9.30	9.25	0.89	18.92	4.32	1.45	20.45	9.65	
inches	0.186	0.505	0.006	0.788	0.786	0.374	0.375	0.045	0.785	0.210	0.067	0.815	0.390	0.010
	0.135	0.495	0.003	0.772	0.774	0.366	0.364	0.035	0.745	0.170	0.057	0.805	0.380	

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B2					03/12/2013

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Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2025/9/22	Rev 1.0	Preliminary Datasheet,

Application data based on LSM-25-28

Notice

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