

250W,50V High Power RF LDMOS FETs

Description

The ITEV05251A2C is a 250watt capable, high performance, internally matched LDMOS FET, designed for RF Energy or ISM application centered at 433MHz, in cost effective 12*10mm QFN plastic package,
It can be soldered on PCB through high density grounding vias or soldered directly on heatsink, according to different applications.

ITEV05251A2C



- Typical CW performance(on Innogrations test board with device soldered on heatsink directly)
50V, Idq=10mA

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
433	53.35	216.5	71.4	21.75	54.1	257.1	74.3

Recommended driver: ITGV22010P3

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DS}	+110	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case $T_C = 85^{\circ}\text{C}$, $T_J = 200^{\circ}\text{C}$, DC test, soldered on heatsink	$R_{\theta JC}$	0.65	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics ($T_A = 25^{\circ}\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Drain-Source Voltage $V_{GS}=0$, $I_{DS}=1.0\text{mA}$	$V_{(BR)DSS}$		110		V
Zero Gate Voltage Drain Leakage Current	I_{DSS}	—	—	1	μA

DC Characteristics (per half section)

ITEV05251A2C LDMOS TRANSISTOR

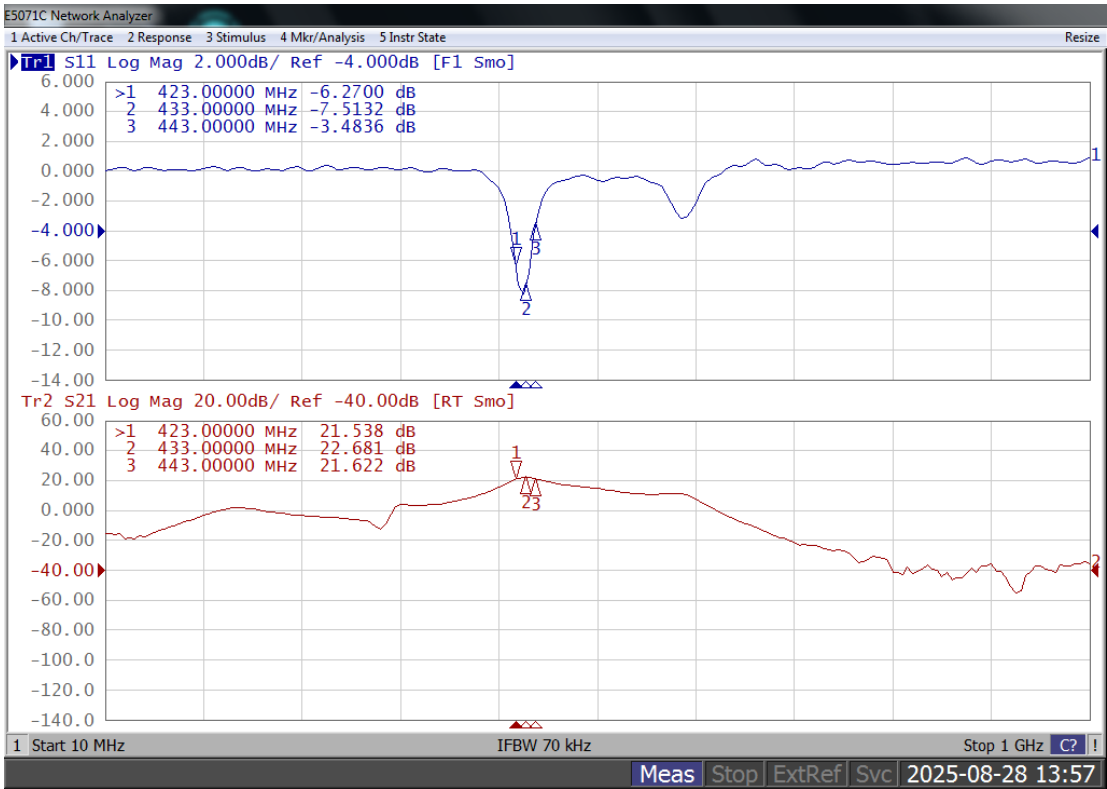
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Preliminary Datasheet V1.0

(V _{DS} = 75V, V _{GS} = 0 V)					
Zero Gate Voltage Drain Leakage Current (V _{DS} = 50V, V _{GS} = 0 V)	I _{loss}	—	—	1	μA
Gate--Source Leakage Current (V _{GS} = 10 V, V _{DS} = 0 V)	I _{gss}	—	—	1	μA
Gate Threshold Voltage (V _{DS} = 50V, I _D = 600 μA)	V _{GS(th)}	—	2.65	—	V
Gate Quiescent Voltage (V _{DD} =50 V, I _D = 500 mA, Measured in Functional Test)	V _{GS(Q)}	—	3.7	—	V

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V _{DD} = 50 Vdc, I _{DQ} = 100 mA, f =433MHz, pulse width:100us, duty cycle:10%	
Load 10:1 All phase angles, at 250W Pulsed CW Output Power	No Device Degradation

TYPICAL CHARACTERISTICS

Figure 2: Network analyzer output S11/221



Reference Circuit of Test Fixture Assembly Diagram

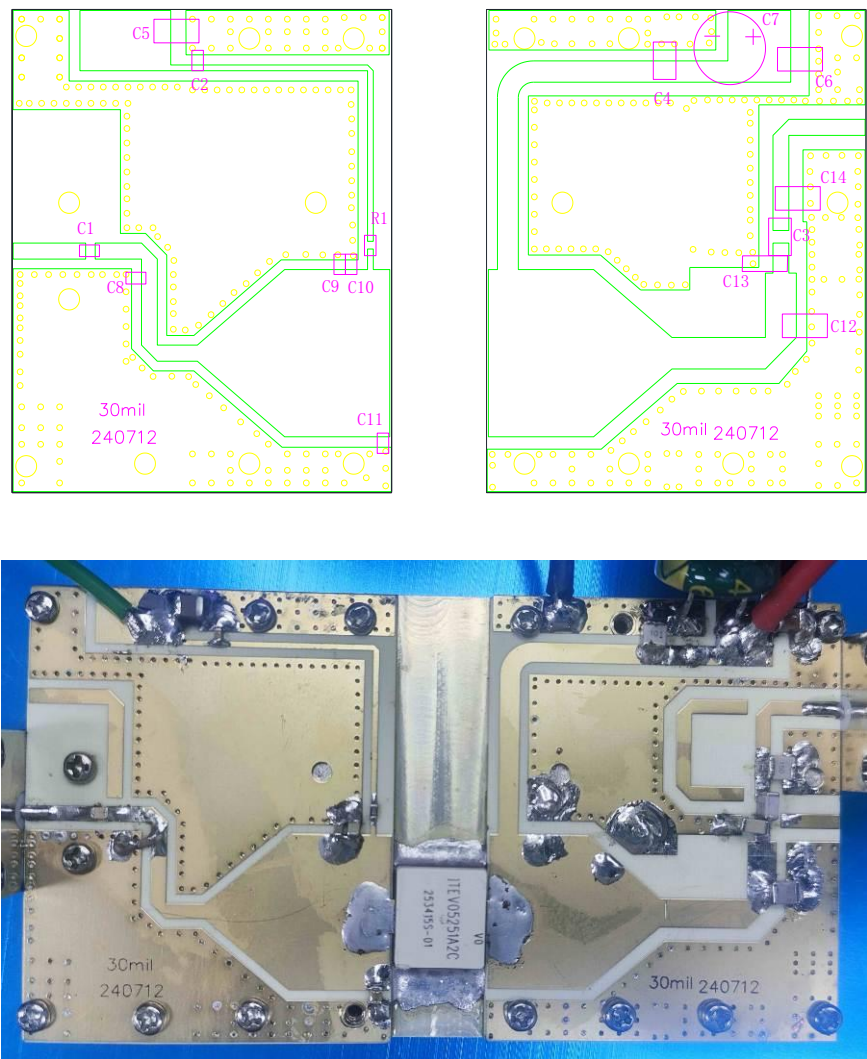


Table 5. Test Circuit Component Designations and Values

Designator	Comment	Footprint	Quantity
C1	3.9 pF/250V	0603/0805	1
C2	100 pF /250V	0603/0805	1
C3, C4	100 pF /250V	1210	2
C5, C6	10 uF/100V	1210	2
C7	1000 uF/63V		1
C8, C9, C10	20 pF/250V	0603/0805	3
C11	30 pF/250V	0603/0805	1
C12	3.9 pF/250V	1210	1
C13	6.8 pF/250V	1210	1
C14	15 pF /250V	1210	1
R1	10 Ω	0603	1

