Document Number: ITEV05251A2C Preliminary Datasheet V1.0

# 250W,50V High Power RF LDMOS FETs

## **Description**

The ITEV05251A2C is a 250watt capable, high performance, internally matched LDMOS FET, designed for RF Energy or ISM application centered at 433MHz, in cost effective 12\*10mm QFN plastic package,

It can be soldered on PCB through high density grounding vias or soldered directly on heatsink, according to different applications.



Typical CW performance(on Innogration test board with device soldered on heatsink directly)
50V, Idq=10mA

Freq	P1dB	P1dB	P1dB	P1dB	P3dB	P3dB	P3dB
(MHz)	(dBm)	(W)	Eff(%)	Gain(dB)	(dBm)	(W)	Eff(%)
433	53.35	216.5	71.4	21.75	54.1	257.1	74.3

Recommended driver: ITGV22010P3

## **Features**

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- · Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

#### **Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
DrainSource Voltage	V <sub>DSS</sub>	+110	Vdc
GateSource Voltage	$V_{GS}$	-10 to +10	Vdc
Operating Voltage	$V_{DD}$	+55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	Tc	+150	°C
Operating Junction Temperature	TJ	+225	°C

#### **Table 2. Thermal Characteristics**

Characteristic	Symbol	Value	Unit	
Thermal Resistance, Junction to Case	Rejc	0.65	°C/W	
T <sub>C</sub> = 85°C, T <sub>J</sub> =200°C, DC test, soldered on heatsink		0.65		

## **Table 3. ESD Protection Characteristics**

Test Methodology	Class	
Human Body Model (per JESD22A114)	Class 2	

## Table 4. Electrical Characteristics (T<sub>A</sub> = 25 °C unless otherwise noted)

Characteristic	Symbol	Min	Тур	Max	Unit
OC Characteristics (per half section)					
Drain-Source Voltage	V		110		V
V <sub>GS</sub> =0, I <sub>DS</sub> =1.0mA	V <sub>(BR)DSS</sub>		110		V
Zero Gate Voltage Drain Leakage Current	I <sub>DSS</sub>			1	μА

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(V <sub>DS</sub> = 75V, V <sub>GS</sub> = 0 V)				
Zero Gate Voltage Drain Leakage Current		 	1	^
$(V_{DS} = 50V, V_{GS} = 0 V)$	I <sub>DSS</sub>	 <del></del>	ı	μΑ
GateSource Leakage Current		 	4	^
$(V_{GS} = 10 \text{ V}, V_{DS} = 0 \text{ V})$	I <sub>GSS</sub>		ı	μΑ
Gate Threshold Voltage	V (45)	 2.65		V
$(V_{DS} = 50V, I_D = 600 \mu A)$	V <sub>GS</sub> (th)	 2.00		V
Gate Quiescent Voltage	V	 3.7		V
(V <sub>DD</sub> =50 V, I <sub>D</sub> = 500 mA, Measured in Functional Test)	$V_{GS(Q)}$	 3.1		V

Load Mismatch (In Innogration Test Fixture, 50 ohm system):  $V_{DD}$  = 50 Vdc,  $I_{DQ}$  = 100 mA, f =433MHz, pulse width:100us, duty cycle:10%

Load 10:1 All phase angles, at 250W Pulsed CW Output Power

No Device Degradation

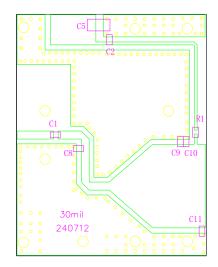
## **TYPICAL CHARACTERISTICS**

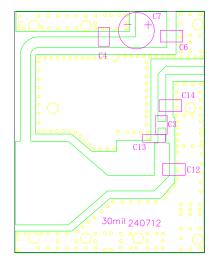


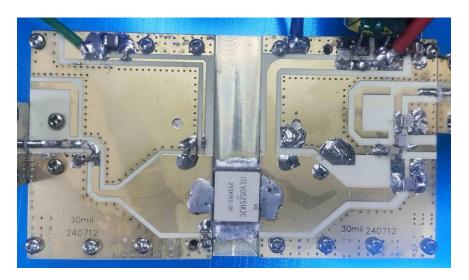


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## **Reference Circuit of Test Fixture Assembly Diagram**





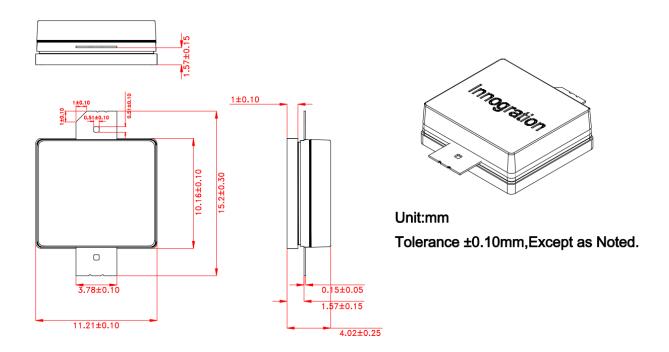


**Table 5. Test Circuit Component Designations and Values** 

		_	
Designator	Comment	Footprint	Quantity
C1	3.9 pF/250V	0603/0805	1
C2	100 pF /250V	0603/0805	1
C3, C4	100 pF /250V	1210	2
C5, C6	10 uF/100V	1210	2
C7	1000 uF/63V		1
C8, C9, C10	20 pF/250V	0603/0805	3
C11	30 pF/250V	0603/0805	1
C12	3.9 pF/250V	1210	1
C13	6.8 pF/250V	1210	1
C14	15 pF /250V	1210	1
R1	10 Ω	0603	1

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## Package Dimensions (Unit:mm)



## **Revision history**

Table 5. Document revision history

Date	Revision	Datasheet Status
2025/9/8 Rev 1.0		Preliminary Datasheet Creation

Application data based on LSM-25-25

### **Disclaimers**

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