



2-6.5GHz, 1W, 28V GaN MMIC PA

Description

The X2IAH2065-1 is a 1-watt, 2 stages GaN MMIC Power Amplifier, designed for ultrawide band, with frequencies from 2 to 6GHz. It is both 50 Ω matched at input and output, requiring minimal external components, offering higher gain and excellent gain flatness



Relative MMIC bare die part number: X2IAH2065-1D

- Typical CW performance Characterization Performance with device soldered

$V_{DS} = 28V$, $I_{DQ} = 14\text{ mA}$ $V_{GS} = -2.70V$

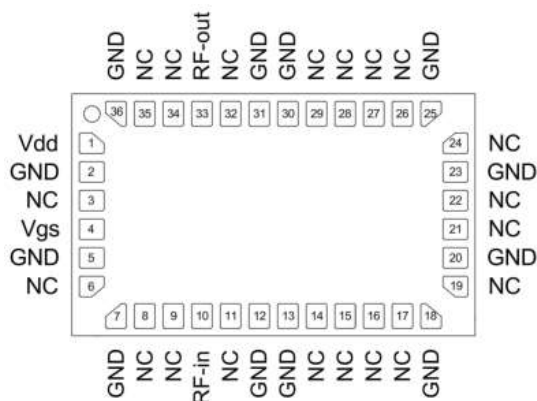
Parameter	2.0GHz	2.5GHz	3.0GHz	4.0GHz	5.0GHz	6.0GHz	6.5GHz	7.0GHz	7.5GHz	Units
Linear Gain	22.2	24.4	25.5	24.4	21.5	22.6	23.2	21.1	19.4	dB
Gain@Pin=9dBm	20.4	22.0	22.6	21.7	20.4	21.1	21.0	19.3	17.8	dB
Pout@Pin=9dBm	0.9	1.2	1.4	1.2	0.9	1.0	1.0	0.7	0.5	W
Eff@Pin=9dBm	21	26	26	22	18	22	21	17	14	%

*P_{sat} to present full band >1W on next pages

Applications

- Power Gain block for Sub-6GHz power amplifier
- Ultrabroad band power amplifier for EMC, instrumentation, and Jammer.
- L, S, C band PA

Pin Configuration and Description



- Top View

Pin No.	Symbol	Description
33	RF-out	Transistor 1, RF Output
10	RF-in	Transistor 1, RF Input
1	Vdd	Transistor 1, Drain Bias
4	Vgs	Transistor 1, Gate Bias
Others	NC	No connection
2,5,7,12, 13,18,20,23,25, 30, 31,36 Package Base	GND	DC/RF Ground. Must be soldered to EVB ground plane over array of vias for thermal and RF performance. Solder voids under Pkg Base will result in excessive junction temperatures causing permanent damage.



Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DS}	150	Vdc
Gate--Source Voltage	V_{GS}	-10 to +2	Vdc
Operating Voltage	V_{DD}	+32	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_c	+150	°C
Operating Junction Temperature	T_j	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case $T_c=25^{\circ}\text{C}$, DC test	$R_{\theta JC}$	20	°C/W

Table 3. Electrical Characteristics

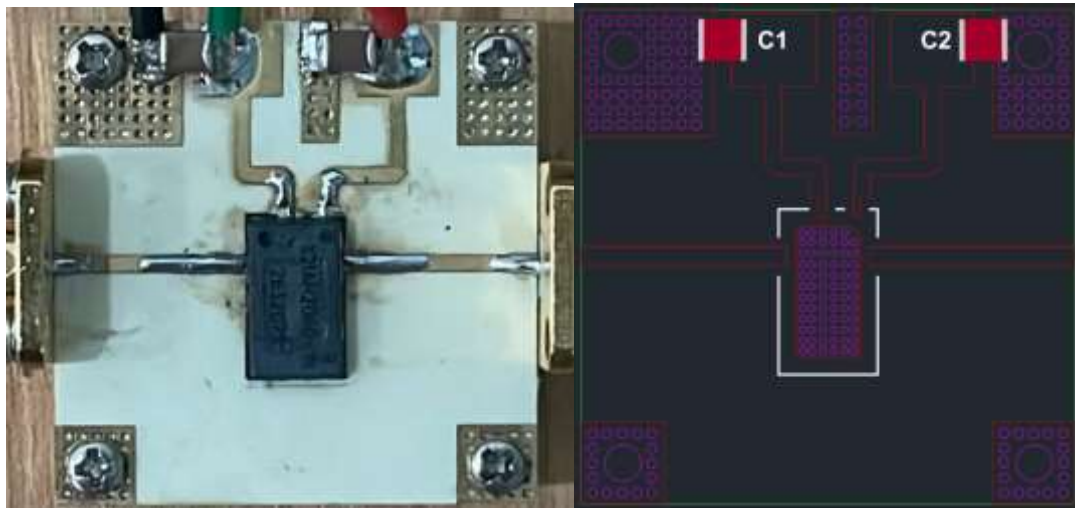
Parameter	Condition	Min	Typ	Max	Unit
Frequency Range		2000		6500	MHz
Power Gain @ Psat		20			dB
P_{SAT}	P4dB	30			dBm
Drain Efficiency @ P_{SAT}		15			%

Unless otherwise noted: $T_A = 25^{\circ}\text{C}$, $V_{DD} = 28\text{ V}$, Pulse Width=100 us, Duty cycle=10%

Load Mismatch of per Section (On Test Fixture, 50 ohm system): $V_{DD} = 28\text{ V}$, $I_{DQ} = 30\text{ mA}$, $f = 3.5\text{ GHz}$

VSWR 10:1 at P3dB pulse CW Output Power	No Device Degradation
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Reference Circuit of Test Fixture Assembly Diagram



		Part NO.	Vendor
C1,C2	10uF 100V Chip Capacitor	C5750X7S2A106M230KB	TDK
PCB	RO4350B,20mil,er=3.48		

Figure Test Circuit Component Layout

TYPICAL CHARACTERISTICS

Figure 3. P3dB Power Gain and, efficiency and Pout @Pin=9dBm vs. Frequency

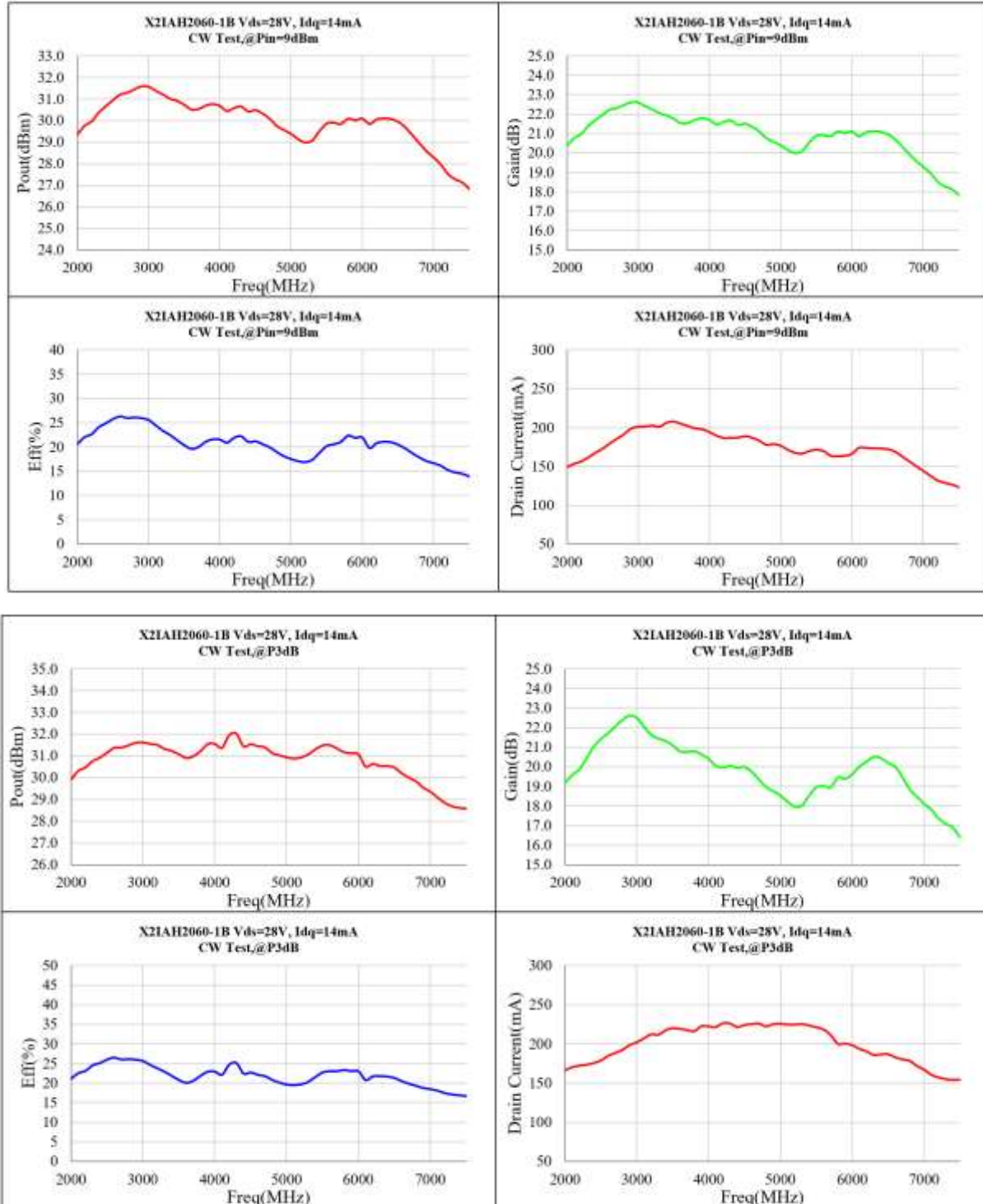
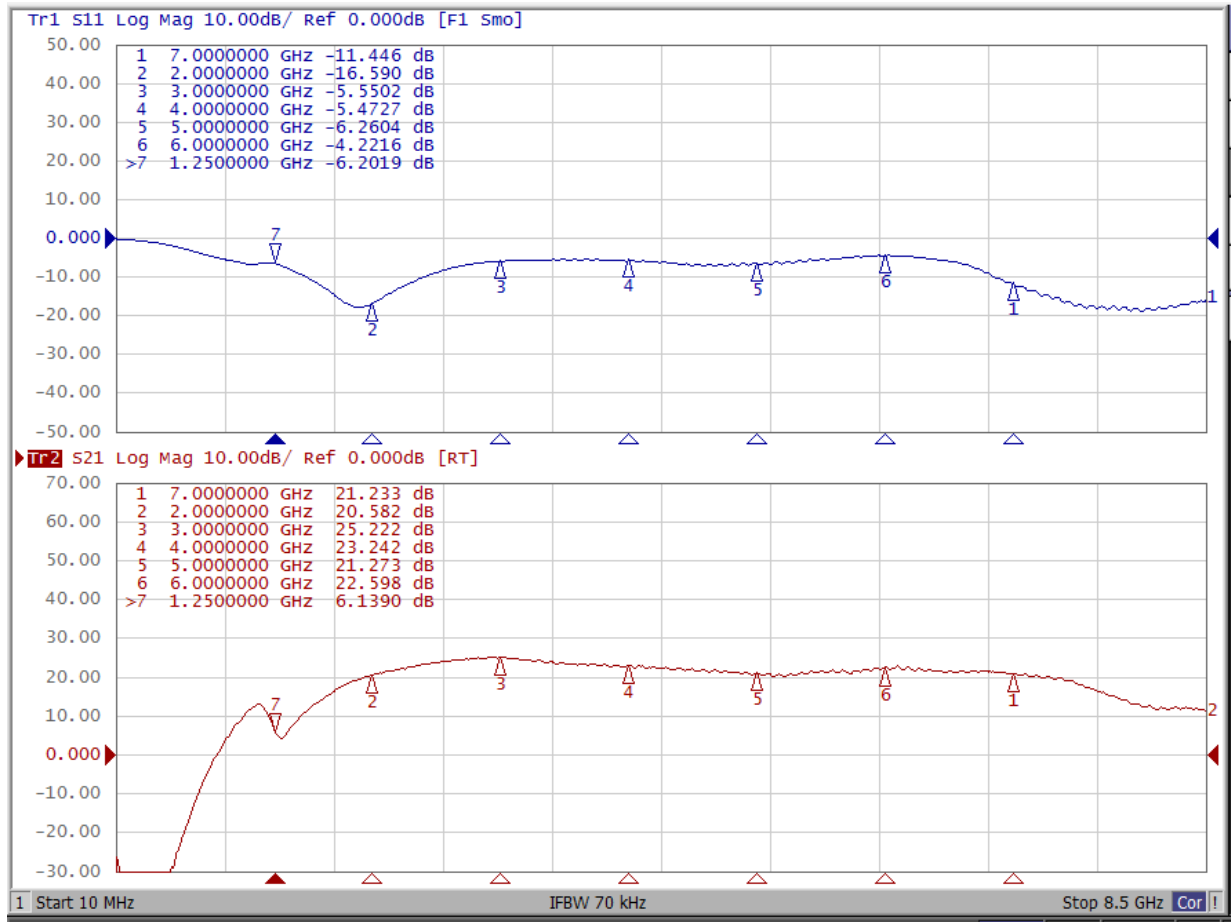




Figure 3. Network analyzer output S11 S21

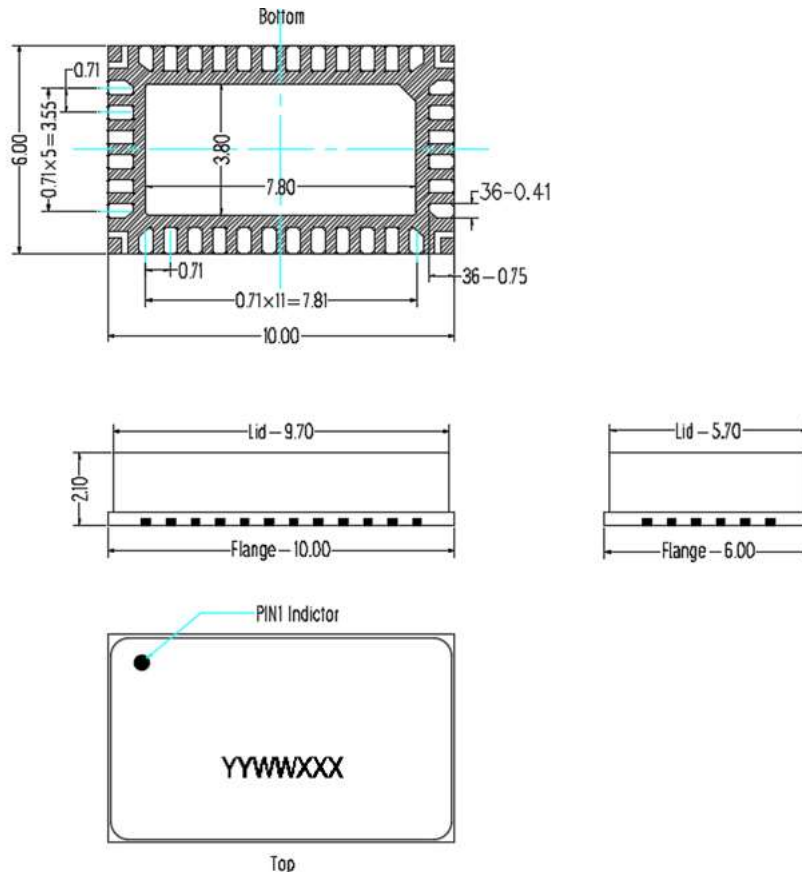
V_{DD} = 28 Vdc, I_{DQ} = 14mA





Package Dimensions

10*6 Plastic Package



Notes:

1. All dimensions are in mm;
2. The tolerances unless specified are ± 0.2 mm.

Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2026/10/10	V1.0	Preliminary Datasheet Creation

Application data based on: ZHH-26-07

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