M2M1505V LDMOS TRANSISTOR

Document Number: M2M1505V
Product Datasheet V1.0

20W, 1GHz General Purpose RF LDMOS FETs

M2M1505V



Description

The M2M1505V is a 20-watt, highly rugged, unmatched LDMOS FET, designed for wide-band commercial and industrial applications at frequencies up to 1 GHz. It can be used in Class AB for all typical modulation formats.

It can support CW, pulsed CW either saturated or linear operation.

It is the ruggedness and stability enhancement of MM2002A mainly at HF to UHF band

- Typical Performance (On Innogration fixture with device soldered):

M2M1505V VDD=28V Vgs=3.35V Idq=100mA CW						
F	Pin	Pout	Pout	IDS	Gain	Eff
MHz	dBm	dBm	(W)	(A)	(dB)	%
170	29.0	43	20.0	1.09	14.0	65.4
190	29.0	43.1	20.4	1.18	14.1	61.8
210	29.0	43.07	20.3	1.24	14.1	58.4
230	29.0	43.38	21.8	1.36	14.4	57.2
250	29.0	44.16	26.1	1.53	15.2	60.8
270	29.0	43.7	23.4	1.41	14.7	59.4
290	29.0	44	25.1	1.44	15.0	62.3
310	29.0	45.15	32.7	1.64	16.2	71.3
330	29.0	44.24	26.5	1.32	15.2	71.8
350	29.0	43.66	23.2	1.11	14.7	74.7
370	29.0	43.2	20.9	0.97	14.2	76.9

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- General purpose power amplifier
- HF to UHF band power amplifier

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+110	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+50	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	$R_{\theta JC}$	1.6	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage V_{GS}=0, I_{DS}=500uA	$V_{(BR)DSS}$		115		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate--Source Leakage Current (V_{GS} = 9 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 28V, I_D = 600 μA)	$V_{GS(th)}$	——	1.98	——	V
Gate Quiescent Voltage (V_{DD} = 28 V, I_D = 50 mA, Measured in Functional Test)	$V_{GS(Q)}$	——	2.53	——	V
Common Source Input Capacitance (V_{GS} = 0V, V_{DS} =28 V, f = 1 MHz)	C_{ISS}		26		pF
Common Source Output Capacitance (V_{GS} = 0V, V_{DS} =28 V, f = 1 MHz)	C_{OSS}		11		pF
Common Source Feedback Capacitance (V_{GS} = 0V, V_{DS} =28 V, f = 1 MHz)	C_{RSS}		0.8		pF

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 28 Vdc, I_{DQ} = 100 mA, f = 1000 MHz

VSWR 10:1 at 20W pulse CW Output Power	No Device Degradation

170-370MHz

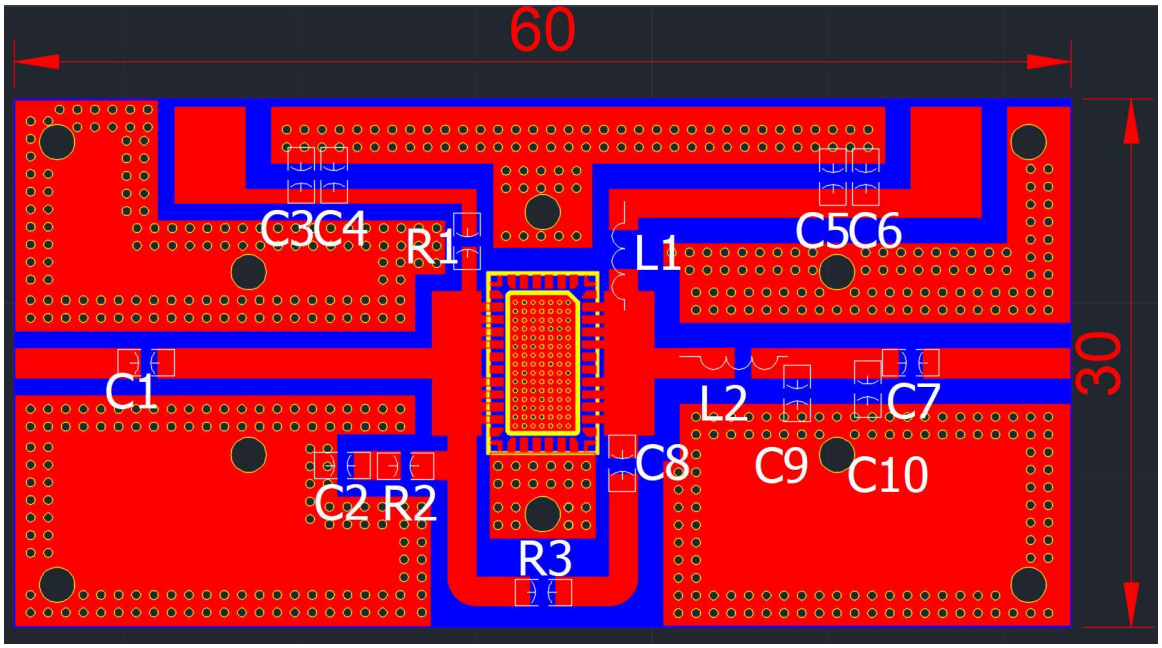
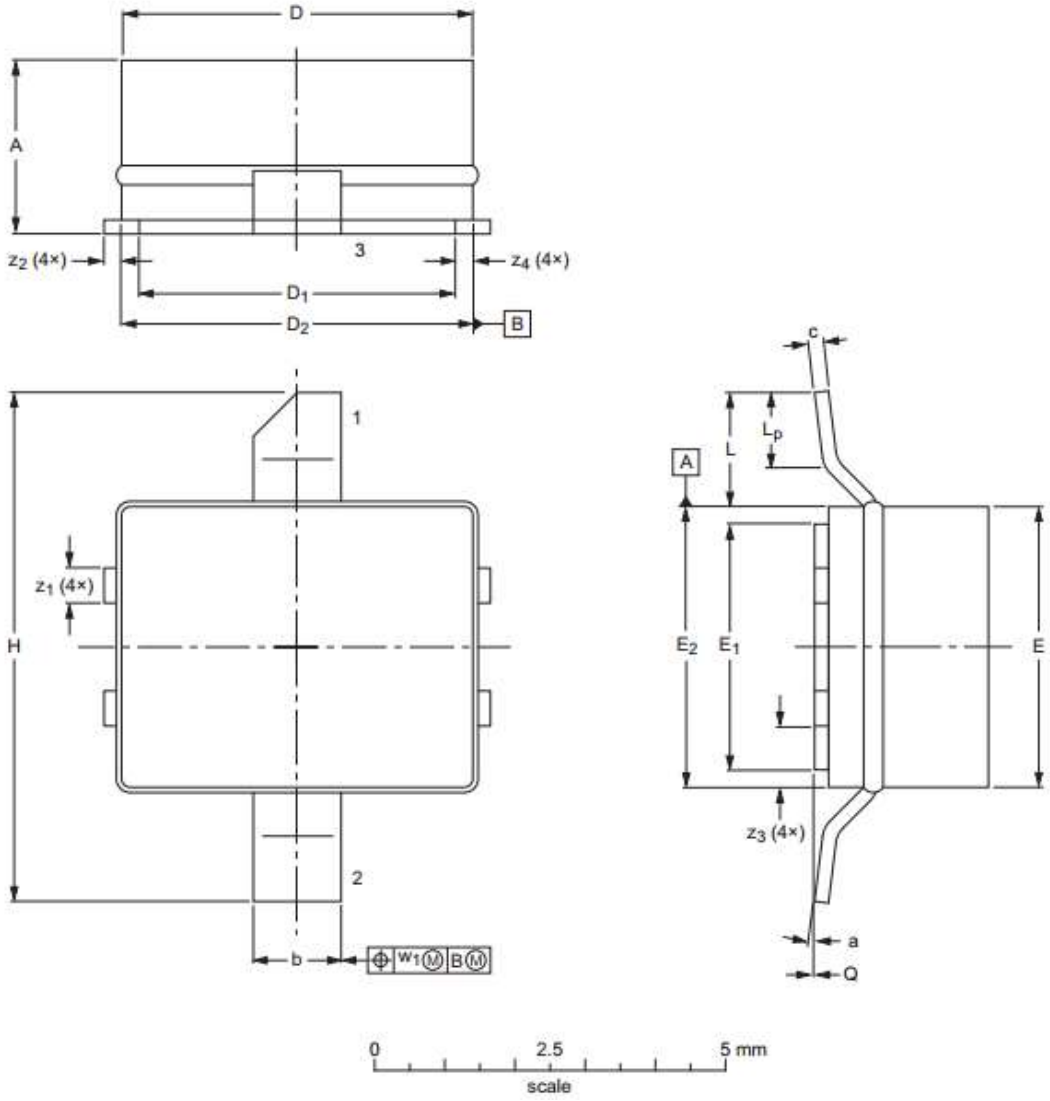


Table 5. Test Circuit Component Designations and Values

Component	Description	Suggested Manufacturer
C2~C3,C6,C8	1uF/200V-0805	
C4,C5	10nF/200V-0805	
C1,C7	910pF	
C9	8.2pF	
10	9.1pF	
R1	300 Ω /1206	Chip Resistor
R2	18 Ω /1206	Chip Resistor
R1	2.2K Ω /1206	Chip Resistor
L1	0.8mm wire 3mm inner diameter, 8Turns；	DIY
L1	0.8mm wire 3mm inner diameter, 2Turns；	DIY

Package Outline

Earless Flanged ceramic package; 2 leads(1-Drain,2-Gate,3-Source)



UNIT	A	b	c	D	D_1	E	E_1	E_2	H	L	L_P	Q	w_1	z_1	z_2	z_3	z_4	α
mm	2.34	1.35	0.23	5.16	4.65	4.14	3.63	4.14	7.49	2.03	1.02	0.1	0.25	0.58	0.25	0.97	0.51	7°
	2.13	1.19	0.18	5.00	4.50	3.99	3.48	3.99	7.24	1.27	0.51	0.0		0.43	0.18	0.81	0.00	0°

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-MM					18/6/2014

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2026/11/2	Rev 1.0	Product Datasheet

Application data based on SYX-26-32

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