

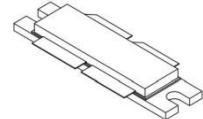
MQ012K1UPX LDMOS TRANSISTOR

Document Number: MQ012K1UPX
Preliminary Datasheet V1.0

1500W/2100W, 50V/60V High Power LDMOS FETs

Description

MQ012K1UPX



The MQ012K1UPX is a 50V/60V 1500W/2100W capable, high performance, unmatched LDMOS FET, designed for commercial and industrial applications with frequencies HF to 225MHz. It can be used for both CW and pulse application.

At popular 50V, It is the ruggedness enhancement of MQ051K5VPX/MQ011K3VPX, and could be the drop-in replacement of BLF188XR/MRFE6VP61K25H.

It is featured for high power and high ruggedness, suitable for Industrial, Scientific and Medical application, as well as FM radio, HF communication, VHF TV and Aerospace applications.

- Typical Performance (On Innogration narrowband fixture with device soldered):

$V_{DD} = 50$ Volts, $I_{DQ} = 200$ mA, CW

Freq(MHz)	Pin(dBm)	Pout(W)	Gain(dB)	Eff(%)
13.56	35	1611	27.2	87

Load mismatch/Ruggedness test, result : **passed**

Freq(MHz)	Signal	VSWR	Pout (W)	Voltage(V)
13.56	CW	70:1 at all phase	1500	50

Features

- High Efficiency and Linear Gain Operations
- On chip RC network enable high stability and ruggedness
- Integrated ESD Protection
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Excellent thermal stability, low HCl drift
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	165	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+60	Vdc
Storage Temperature Range	T_{STG}	-65 to +150	°C
Case Operating Temperature	T_c	+150	°C
Operating Junction Temperature	T_j	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case ,Case Temperature 85°C, 1500W CW, 50 Vdc, $I_{DQ} = 70$ mA	$R_{\theta JC}$	0.12	°C/W
Transient thermal impedance from junction to case $T_j = 150$ °C; $t_p = 100$ us; Duty cycle = 20 %	Z_{th}	0.02	°C/W

Table 3. ESD Protection Characteristics

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Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 °C unless otherwise noted)

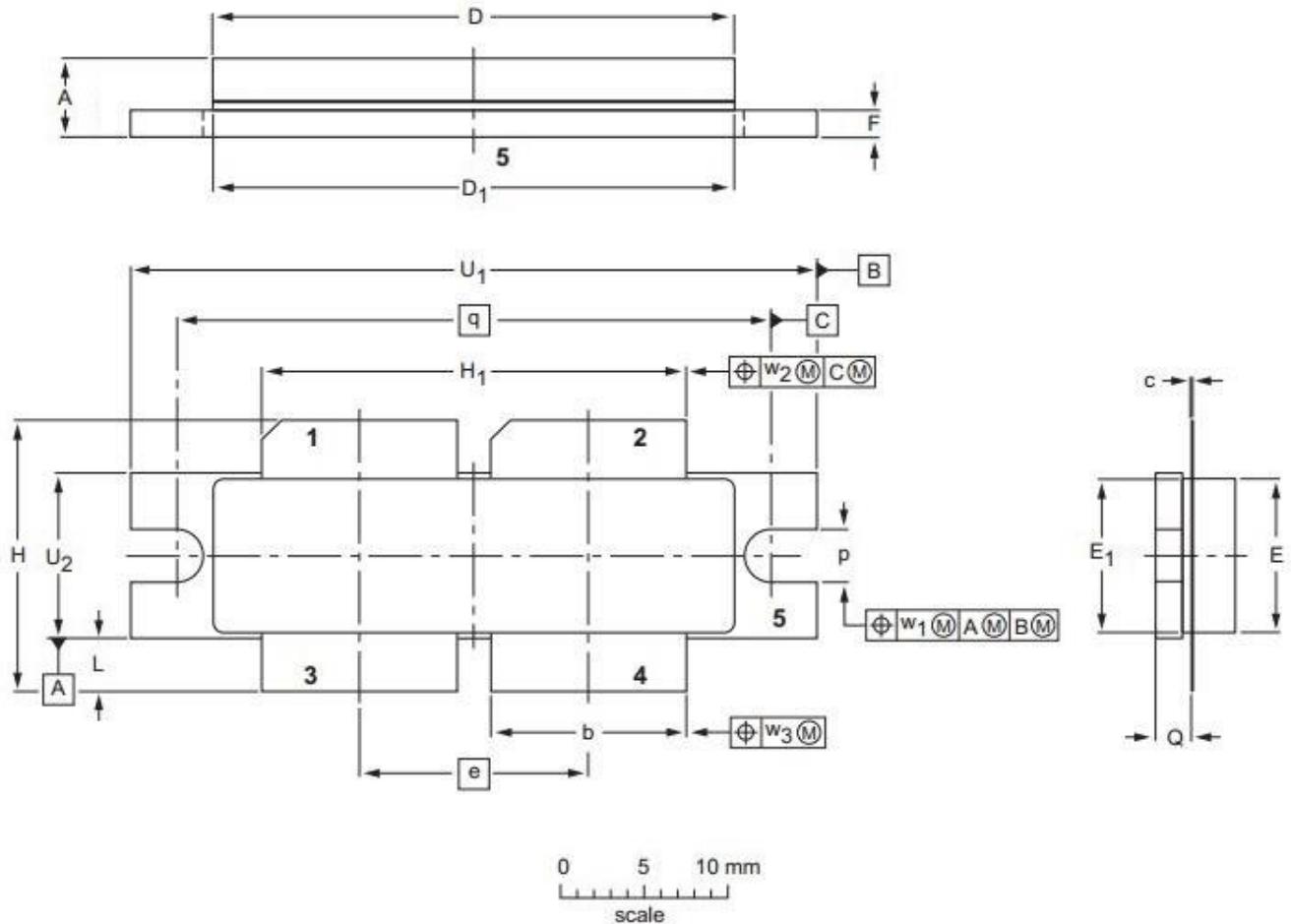
Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage (V _{GS} =0, I _{DS} =20.0mA)	V _{(BR)DSS}		165		V
Zero Gate Voltage Drain Leakage Current (V _{DS} = 50V, V _{GS} = 0 V)	I _{DSS}	—	—	1	µA
Gate—Source Leakage Current (V _{GS} = 10 V, V _{DS} = 0 V)	I _{GSS}	—	—	1	µA
Gate Threshold Voltage (V _{DS} = 50V, I _D = 600 µA)	V _{GS(th)}	—	2.54	—	V
Gate Quiescent Voltage (V _{DD} = 50 V, I _D = 70 mA, Measured in Functional Test)	V _{GS(Q)}	—	3	—	V
Drain source on state resistance (V _{DS} = 0.1V, V _{GS} = 10 V) Each section side of device measured	R _{ds(on)}		85		mΩ
Common Source Input Capacitance (V _{GS} = 0V, V _{DS} =50 V, f = 1 MHz) Each section side of device measured	C _{iss}		1300		pF
Common Source Output Capacitance (V _{GS} = 0V, V _{DS} =50 V, f = 1 MHz) Each section side of device measured	C _{oss}		330		pF
Common Source Feedback Capacitance (V _{GS} = 0V, V _{DS} =50 V, f = 1 MHz) Each section side of device measured	C _{rss}		4.2		pF

Package Outline

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Flanged ceramic package; 2 mounting holes; 4 leads (1, 2—DRAIN, 3, 4—GATE, 5—SOURCE)



UNIT	A	b	c	D	D ₁	e	E	E ₁	F	H	H ₁	L	p	Q	q	U ₁	U ₂	W ₁	W ₂	W ₂
mm	4.7	11.81	0.18	31.55	31.52	13.72	9.50	9.53	1.75	17.12	25.53	3.48	3.30	2.26	35.56	41.28	10.29	0.25	0.51	0.25
	4.2	11.56	0.10	30.94	30.96		9.30	9.27	1.50	16.10	25.27	2.97	3.05	2.01		41.02	10.03			
inches	0.185	0.465	0.007	1.242	1.241	0.540	0.374	0.375	0.069	0.674	1.005	0.137	0.130	0.089	1.400	1.625	0.405	0.01	0.02	0.01
	0.165	0.455	0.004	1.218	1.219		0.366	0.365	0.059	0.634	0.995	0.117	0.120	0.079		1.615	0.395			

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-D4E					03/12/2013

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Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2026/1/22	Rev 1.0	Preliminary Datasheet

Application data based on SYX-26-05

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