

STCV161K3BY2 GaN TRANSISTOR

Document Number: STCV161K3BY2
Preliminary Datasheet V1.0

GaN HEMT 50V, 1300W, RF Power Transistor

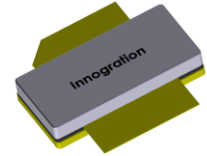
Description

The STCV161K3BY2 is a 1300-watt, internally matched GaN HEMT, designed for pulsed amplifier applications with frequencies at 1575MHz.

When used at higher voltage up to 60V, it can deliver 1600W

It is recommended to use this device only at pulse condition, and power rating might vary according to different pulse width and duty cycle

STCV161K3BY2



- Typical **pulse** STCV161K3BY2 (On Innogration fixture with device soldered):

$V_{DD} = 50$ Volts, $I_{DQ} = 100$ mA, Pulse CW, Pulse width=20us, Duty cycle=10%.

Vds (V)	Freq (MHz)	P2dB (dBm)	P2dB (W)	P2dB Eff(%)	P2dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
50V	1575	60.97	1251.1	68.3	16.62	61.15	1302.7	69.4
55V	1575	61.68	1472.5	67.3	16.81	61.75	1496.1	67.8
60V	1575	62.16	1645.1	64.9	16.86	62.18	1653.7	65.5

Applications and Features

- Suitable for high power pulsed RF Energy application in L band avionics
- Thermally Enhanced Industry Standard Package
- High Reliability Metallization Process
- Excellent thermal Stability and Excellent Ruggedness
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

■ Turning the device ON

- 1) Set VGS to the pinch-off (VP) voltage, typically -5 V
- 2) Turn on VDS to nominal supply voltage (50 V)
- 3) Increase VGS until IDS current is attained
- 4) Apply RF input power to desired level

■ Turning the device OFF

- 1) Turn RF power off
- 2) Reduce VGS down to VP, typically -5 V
- 3) Reduce VDS down to 0 V
- 4) Turn off VGS

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DS}	+200	Vdc
Gate--Source Voltage	V_{GS}	-8 to +0	Vdc
Operating Voltage	V_{DD}	0 to 60	Vdc
Maximum Forward Gate Current @ $T_C = 25^{\circ}\text{C}$	I_{gmax}	162	mA
Storage Temperature Range	T_{stg}	-65 to +150	$^{\circ}\text{C}$
Case Operating Temperature	T_C	+150	$^{\circ}\text{C}$

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Operating Junction Temperature	T_J	+225	°C
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Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case, $P_{OUT}=1300W$ @1.575GHz 20us/10%, $T_{case}=85^{\circ}C$, 50 Vdc, $I_{DQ}=100\text{ mA}$	$R_{\theta JC}$	0.18	°C/W

Table 3. Electrical Characteristics ($T_A = 25^{\circ}C$ unless otherwise noted)

DC Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS}=-8V$; $I_{DS}=162mA$	V_{DSS}	---	200	---	V
Gate Threshold Voltage	$V_{DS}=10V$, $I_D=162mA$	$V_{GS(th)}$	-4		-2	V
Gate Quiescent Voltage	$V_{DS}=50V$, $I_{DS}=100mA$, Measured in Functional Test	$V_{GS(Q)}$	---	-3.2	---	V

Functional Tests (In Innogration Test Fixture, 50 ohm system) : $V_{DD}=50Vdc$, $I_{DQ}=100\text{ mA}$, $f=1575MHz$, Pulse CW, Pulse width=20us, Duty cycle=20%.

Characteristic	Symbol	Min	Typ	Max	Unit
Power Gain @ P_{-3dB}	G_P	---	15	---	dB
Drain Efficiency@ P_{SAT}	η_D	---	65	---	%
Saturated Power(P_{-3dB})	P_{SAT}	---	61.1	---	dBm
Input Return Loss	IRL	---	-5	---	dB

Load Mismatch (In Innogration Test Fixture, 50 ohm system): $V_{DD}=50\text{ Vdc}$, $I_{DQ}=100\text{ mA}$, $f=1575\text{ MHz}$

VSWR 10:1 at 1300W pulse CW Output Power	No Device Degradation
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TYPICAL CHARACTERISTICS

Figure 2. Test Circuit Component Layout

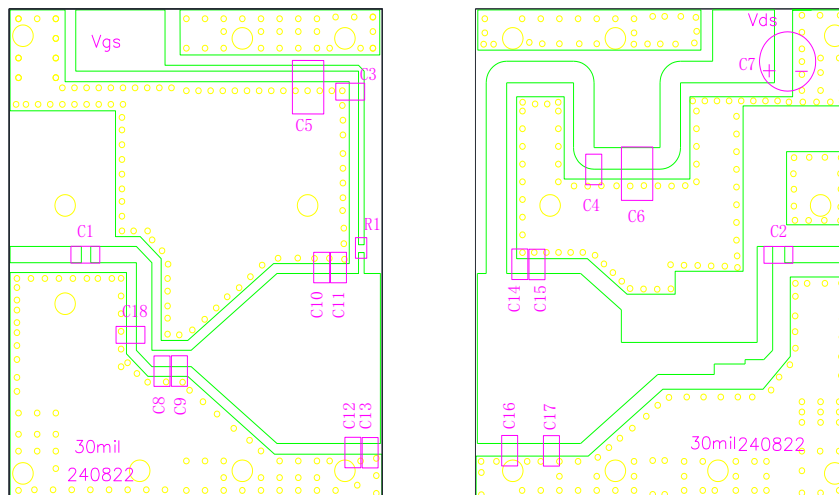


Table 4. Test Circuit Component Designations and Values

Designator	Comment	Footprint	Quantity
C1	6.8 pF	0603/0805	1
C2, C3, C4,	30 pF	0805	3
C5, C6	10uF/100V	1210	2
C7	1000uF/63V		1
C8, C10, C11, C12, C13	2.7 pF	0603/0805	5
C9, C18	1.5 pF	0603/0805	2
C14	3.0 pF	0805	1
C15	1.0 pF	0805	1
C16, C17	3.3 pF	0805	2
R1	10 Ω	0603	1

TYPICAL CHARACTERISTICS

Figure 1: Efficiency and power gain as function of Pout

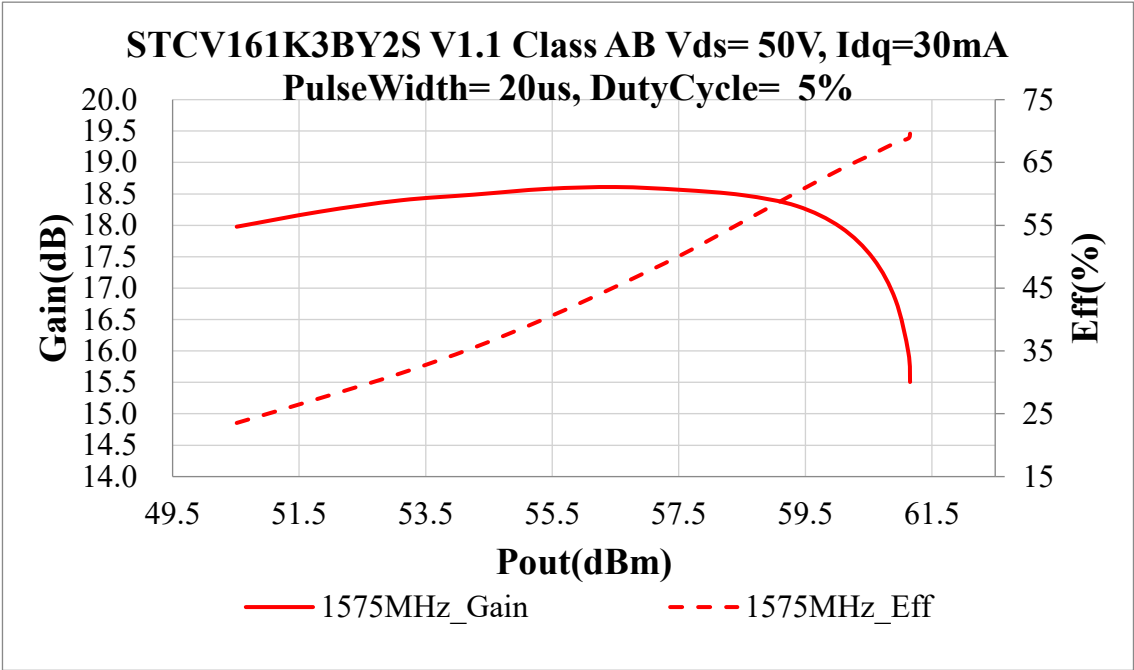


Figure 2: S11/S21 output from Network analyser

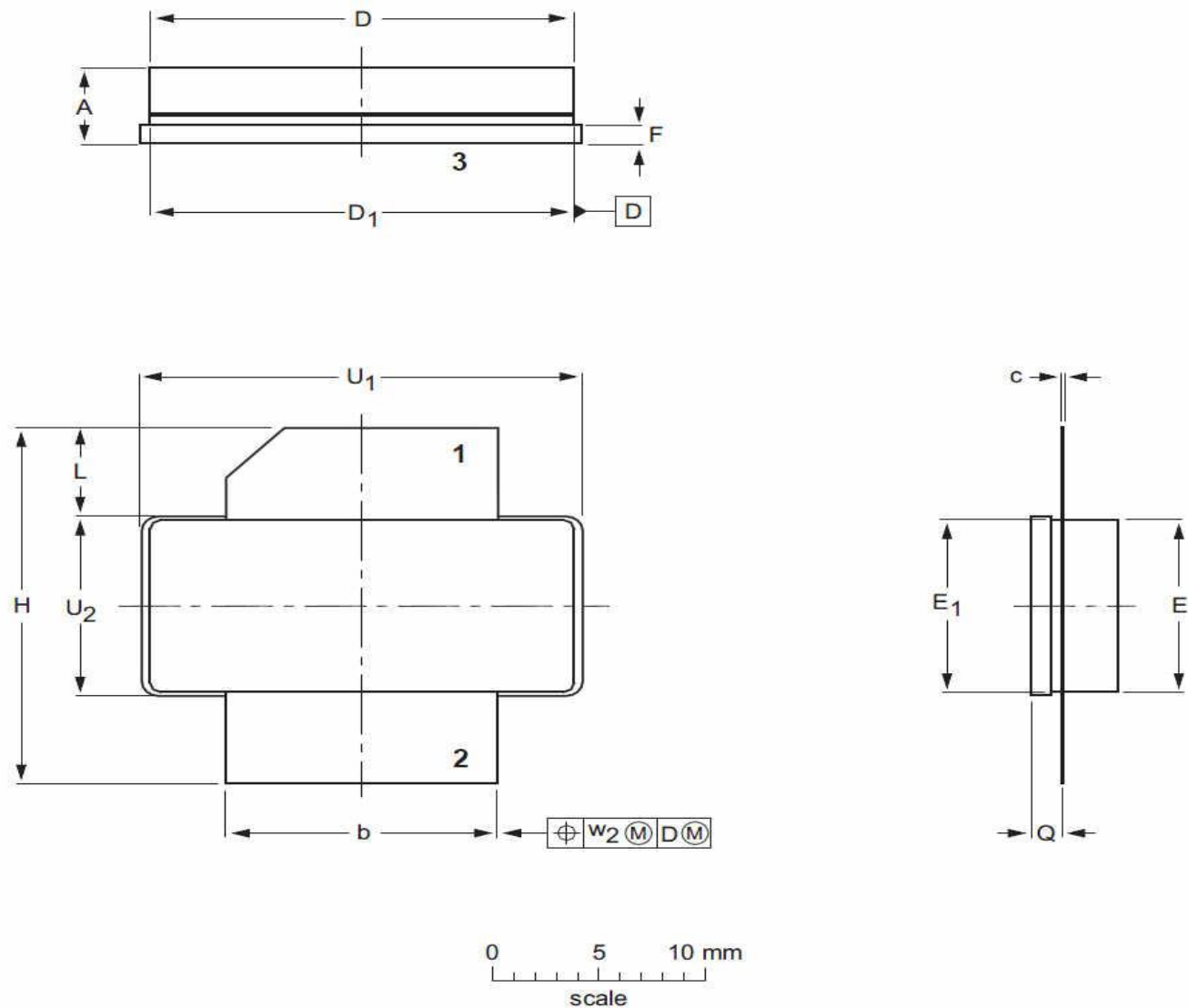


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Package Outline

Earless flanged ceramic package; 2 leads (1—DRAIN、2—GATE、3—SOURCE)



UNIT	A	b	c	D	D ₁	E	E ₁	F	H	L	Q	U ₁	U ₂	W ₂
mm	4.72	12.83	0.15	20.02	19.96	9.50	9.53	1.14	19.94	5.33	1.70	20.70	9.91	0.25
	3.43	12.57	0.08	19.61	19.66	9.30	9.25	0.89	18.92	4.32	1.45	20.45	9.65	
inches	0.186	0.505	0.006	0.788	0.786	0.374	0.375	0.045	0.785	0.210	0.067	0.815	0.390	0.010
	0.135	0.495	0.003	0.772	0.774	0.366	0.364	0.035	0.745	0.170	0.057	0.805	0.380	

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B2					03/12/2013

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Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2026/1/26	Rev 1.0	Preliminary Datasheet,

Application data based on LSM-26-03

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