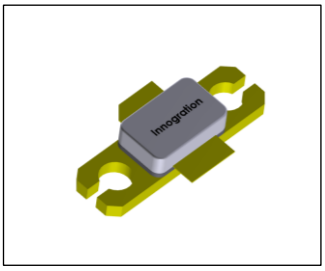
GaN HEMT 28V, HF-2.5GHz 220W, RF Power Transistor



Description

The XTAH25220GX is a 220W GaN HEMT, input prematched,designed for multiple application up to 2.5GHz It can be used in CW, Pulse and any other modulation modes. There is no guarantee of performance when this part is used in applications designed outside of these frequencies.

- Typical class AB 1500-1600MHz RF Performance with device soldered

  Vds=28V, Idq=400mA，**CW**

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P2.5dB (dBm)	P2.5dB (W)	P2.5dB Eff(%)
1500	52.56	180.3	50.3	13.02	54.66	272.5	61.5
1550	53.22	210.1	58.0	13.2	54.65	272.0	66.4
1600	52.69	185.8	60.4	13.41	53.98	250.3	68.0

- Typical class AB 2300-2350MHz RF Performance with device soldered

  Vds=28V, Idq=300mA，**Pulsed CW， 10us， 10%**

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P2.5dB (dBm)	P2.5dB (W)	P2.5dB Eff(%)
2300	52.43	175.1	50.1	14.8	54.27	267.2	58.6
2350	51.52	142.0	51.9	15.5	53.43	220.3	60.7

Applications

- S band power amplifier
- L band power amplifier
- ISM/RF Energy power amplifier

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

Turning the device ON

1. Set VGS to the pinch--off (VP) voltage, typically –5 V
2. Turn on VDS to nominal supply voltage
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically –5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+200	Vdc
Gate--Source Voltage	V_{GS}	-8 to +0.5	Vdc
Operating Voltage	V_{DD}	50	Vdc
Maximum gate current	Igs	63	mA
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case by FEA T_C= 85°C, at Pdiss=130W	$R_{\theta JC}$	0.9	°C /W

Table 3. Electrical Characteristics (TA = 25℃ unless otherwise noted)

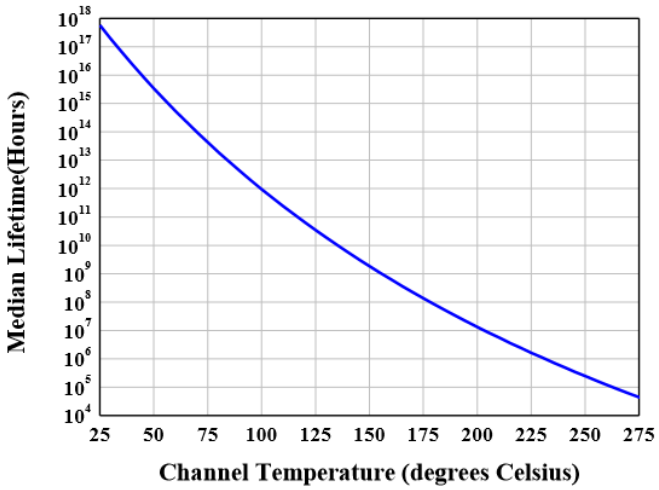
DC Characteristics (measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	VGS=-8V; IDS=63mA	V_{DSS}		200		V
Gate Threshold Voltage	VDS =10V, ID = 63mA	$V_{GS(th)}$	-4		-2	V
Gate Quiescent Voltage	VDS =28V, IDS=400mA, Measured in Functional Test	$V_{GS(Q)}$		-3.1		V

Ruggedness Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Load mismatch capability	1.5GHz, Pout=220W Pulsed CW All phase, No device damages	VSWR		10:1		

Figure 2: Median Lifetime vs. Channel Temperature



1.5-1.6GHz
Typical performance

Figure 2: Network analyzer output S11/S21

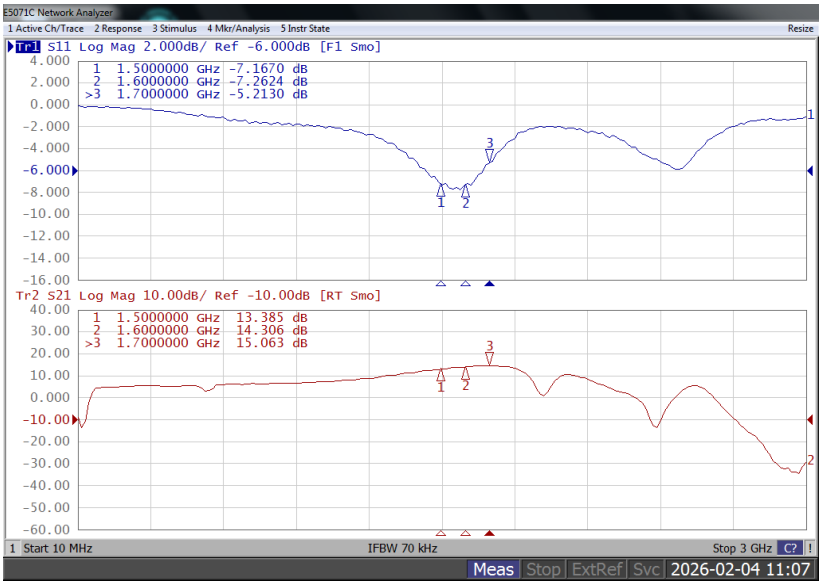


Figure 3: Power efficiency and gain as function of Pout

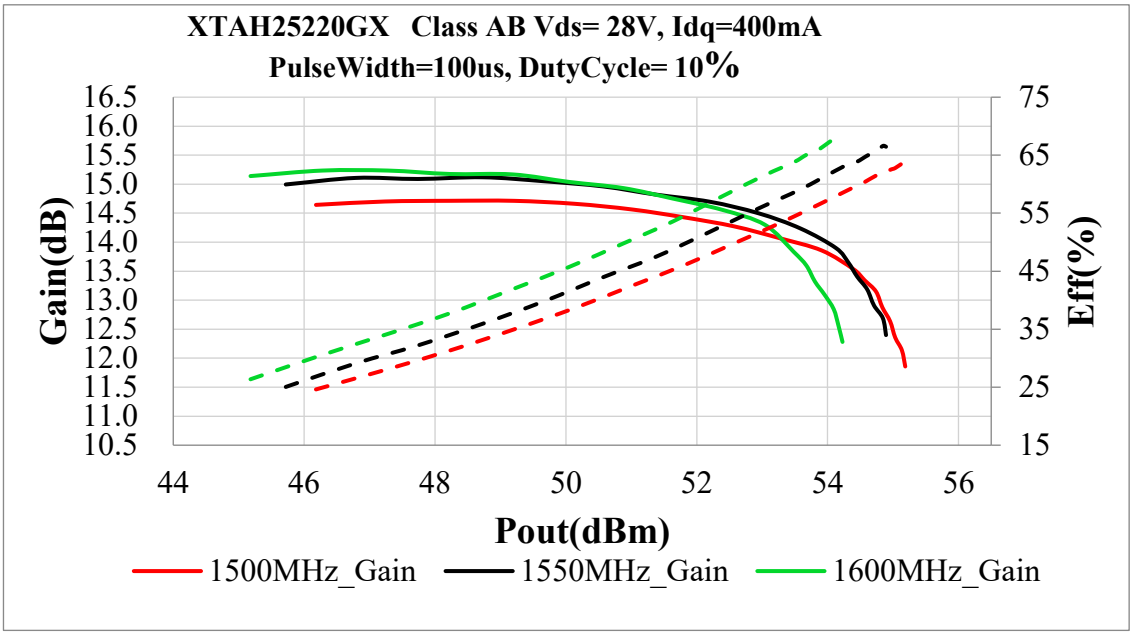
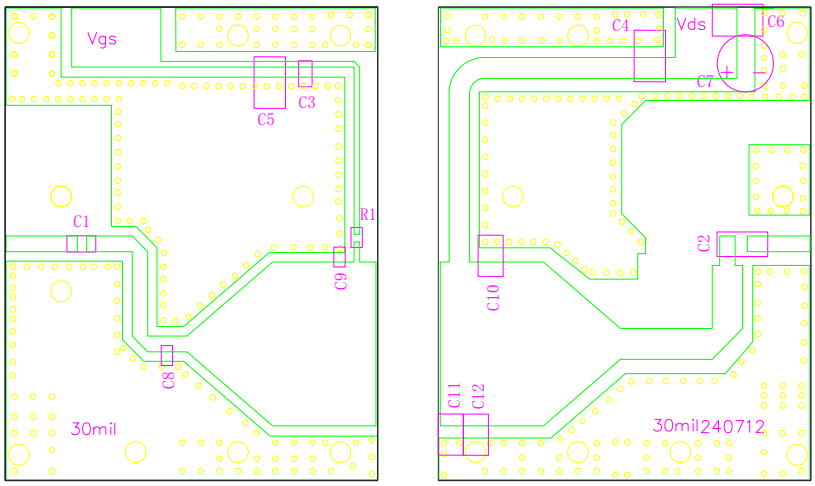


Figure 4: Picture of application board



Designator	Comment	Footprint	Quantity
C1	6.8 pF	0603/0805	1
C2, C4,	30 pF	1210	2
C3	30 pF	0603/0805	1
C5, C6	10uF/100V	1210	2
C7	470uF/63V		1
C8	1.5 pF	0603/0805	1
C9	2.4 pF	0603/0805	1
C10, C11	2.4 pF	1210	2
C12	1.0 pF	1210	1
R1	10 Ω	0603	1

2.3-2.35GHz
Typical performance

Figure 5: Network analyzer output S11/S21

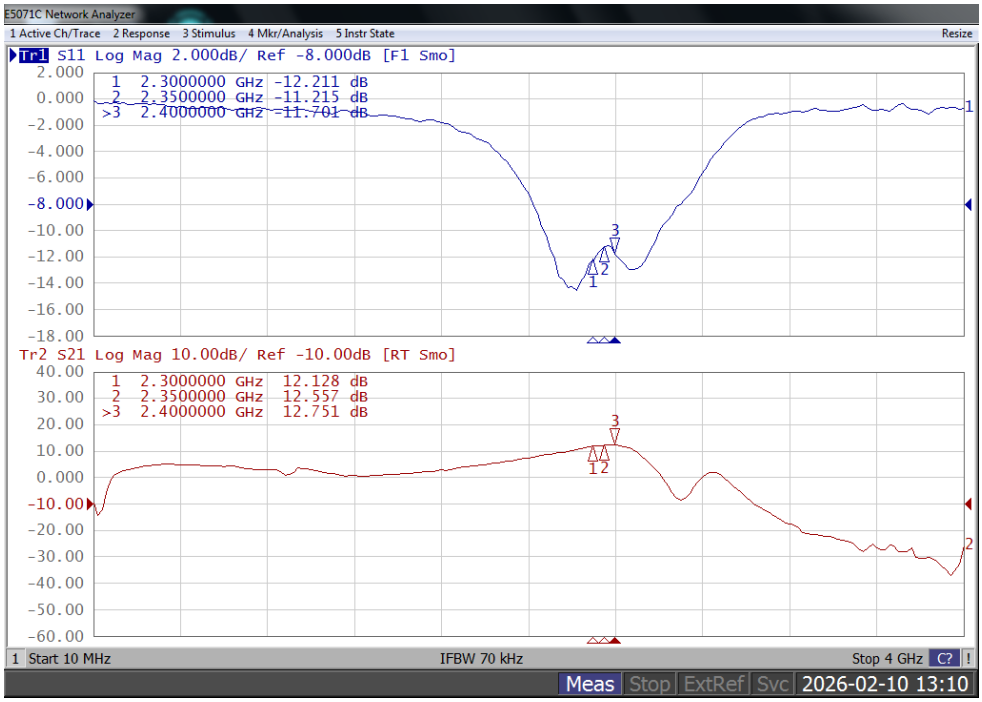


Figure 6: Power efficiency and gain as function of Pout

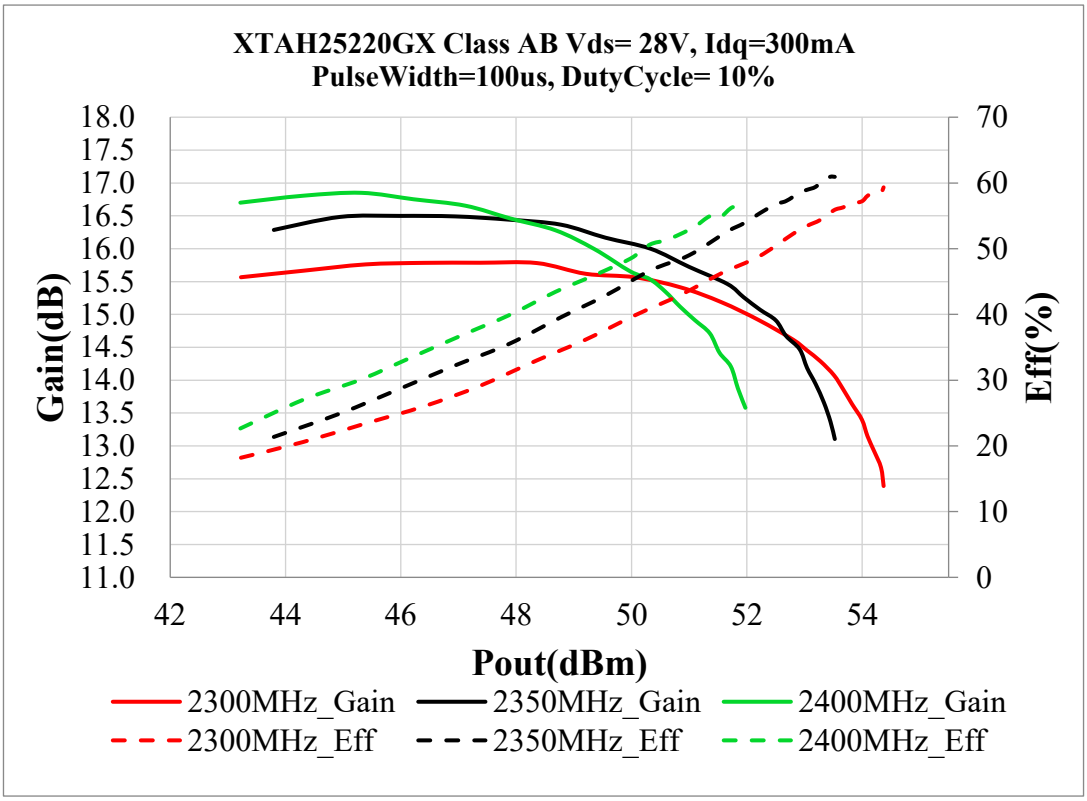
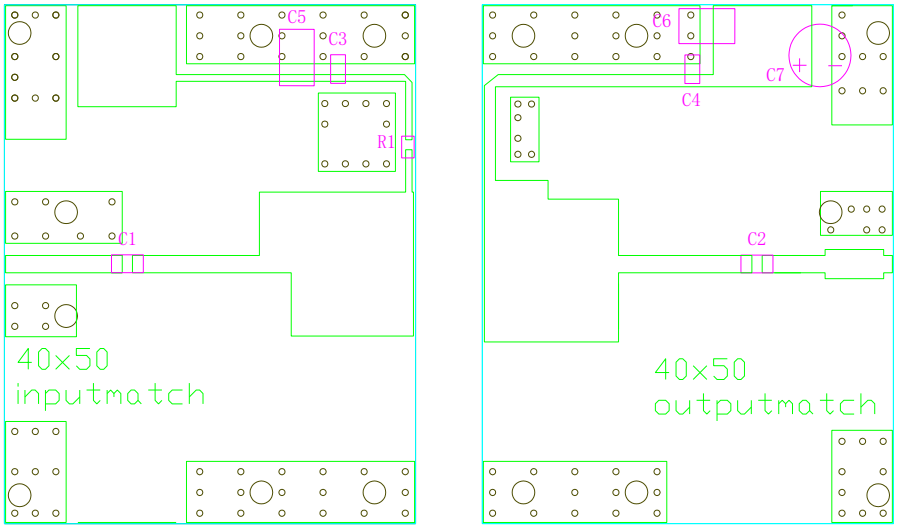


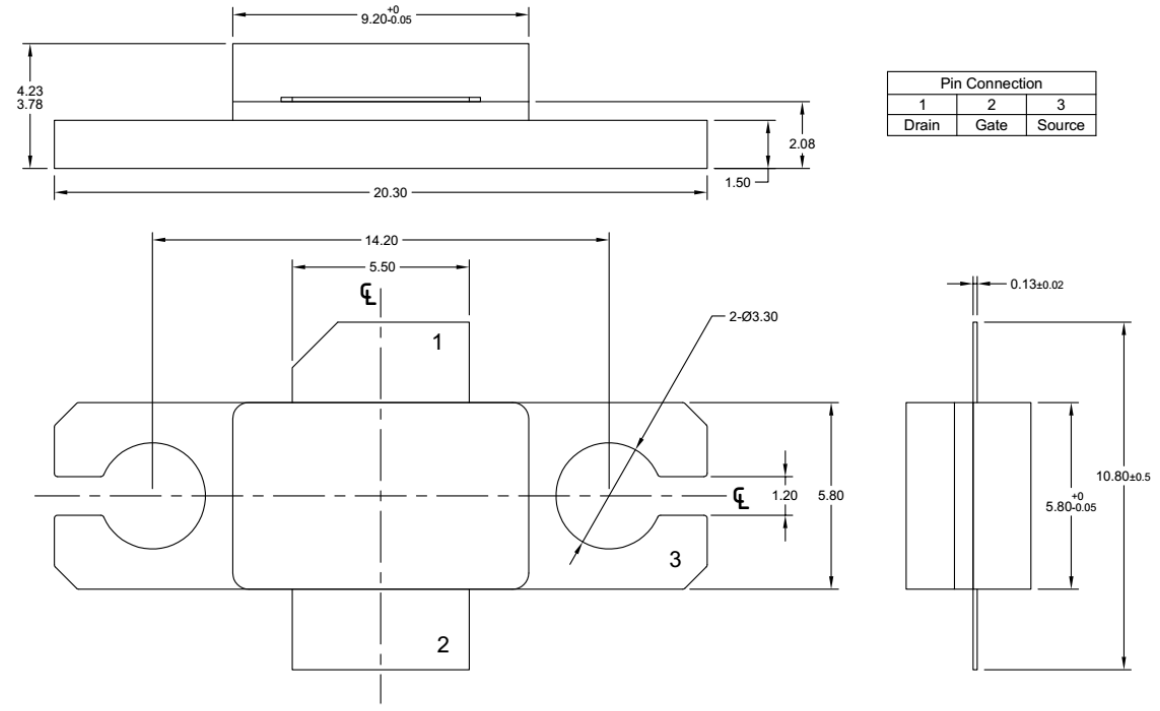
Figure 7: Picture of application board



Designator	Comment	Footprint	Quantity
C1, C2, C3, C4	10 pF	0603/0805	4
C5, C6	10uF/100V	1210	2
C7	470uF/63V		1
R1	10 Ω	0603	1

Package Outline

Flanged ceramic package; 2 leads



Pin Connection		
1	2	3
Drain	Gate	Source

Unit: mm
Tolerances(unless specified): x.x ±0.1
x.xx ±0.05

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-GXB					10/10/2017

Figure 1. Package Outline PKG-G2E

Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2026/2/10	V1.0	Preliminary Datasheet Creation

Application data based on: LSM-26-04/05

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