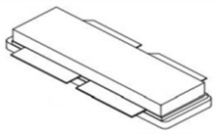
GaN 50V, 750W, L band CW RF Power Transistor

STCV18750RD4



Description

The STCV18750RD4 is a push pull 750W saturated power capable, internally matched GaN HEMT, ideal for ISM or RF energy applications at fixed frequency point or very narrow band within 1.6 to 1.8GHz typically for 1.7G particle accelerator applications.

There is no guarantee of performance when this part is used outside of stated frequencies.

- Typical CW performance at 1.6-1.8GHz applications with transistor soldered on heatsink

STCV18750RD4^{V1} VGS=-3.33V VDS=50V IDQ=150mA CW								
Freq (MHz)	**Psat (dBm)**	**Psat (W)**	**IDS (A)**	**Pin (dBm)**	**Gain (dB)**	**Eff(%)**	**2nd（dBc）**	**3rd（dBc）**
1600	59.10	812.8	25.00	45.00	14.10	66	-47.20	-29.10
1650	59.20	831.8	24.67	44.93	14.27	68	-46.60	-20.80
1700	58.94	783.4	22.77	44.77	14.17	69	-42.60	-32.60
1750	58.59	722.8	20.36	44.44	14.15	71	-31.60	-30.30
1800	58.06	639.7	18.23	44.03	14.03	70	-29.10	-26.00

Applications

- 1.7GHz particle linear accelerator
- L band power amplifier
- GPS ground station

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

Turning the device ON

1. Set VGS to the pinch--off (VP) voltage, typically –5 V
2. Turn on VDS to nominal supply voltage
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically –5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+200	Vdc
Gate--Source Voltage	V_{GS}	-8 to +0.5	Vdc
Operating Voltage	V_{DD}	55	Vdc
Maximum gate current	Igs	102	mA
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case by FEA	$R_{\theta JC}$	0.45	°C /W

T_C= 25°C, at Pd=250W			

Table 3. Electrical Characteristics (TA = 25℃ unless otherwise noted)

DC Characteristics (Each path, measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	VGS=-8V; IDS=51mA	V_{DSS}		200		V
Gate Threshold Voltage	VDS =10V, ID = 51mA	$V_{GS(th)}$	-4	-	-2	V
Gate Quiescent Voltage	VDS =50V, IDS=150mA, Measured in Functional Test	$V_{GS(Q)}$		--3.3		V

Ruggedness Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Load mismatch capability	1.7GHz, Pout=750W pulse CW All phase, No device damages	VSWR		5:1		

TYPICAL CHARACTERISTICS

1600-1800MHz

Figure 1: S11/S21 output from Network analyser (VDS= 50V, IDQ=590 mA Vgs =-3.05V)

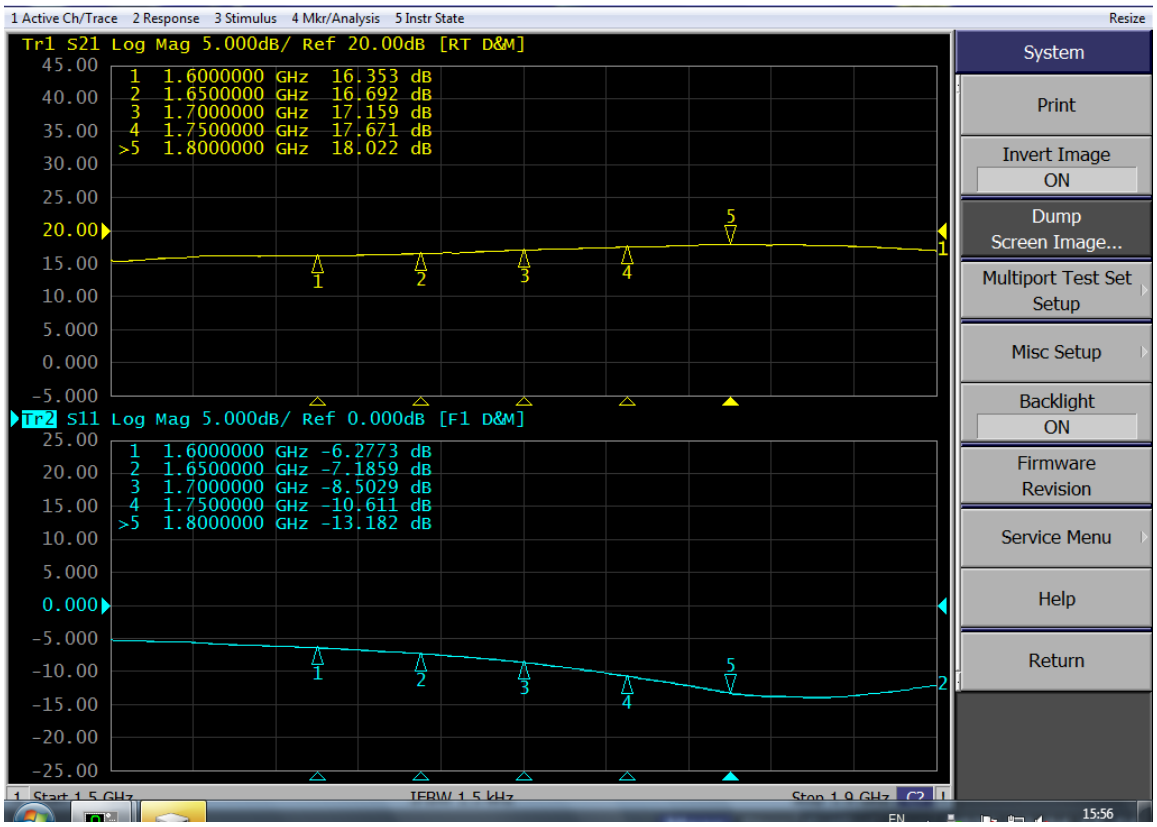
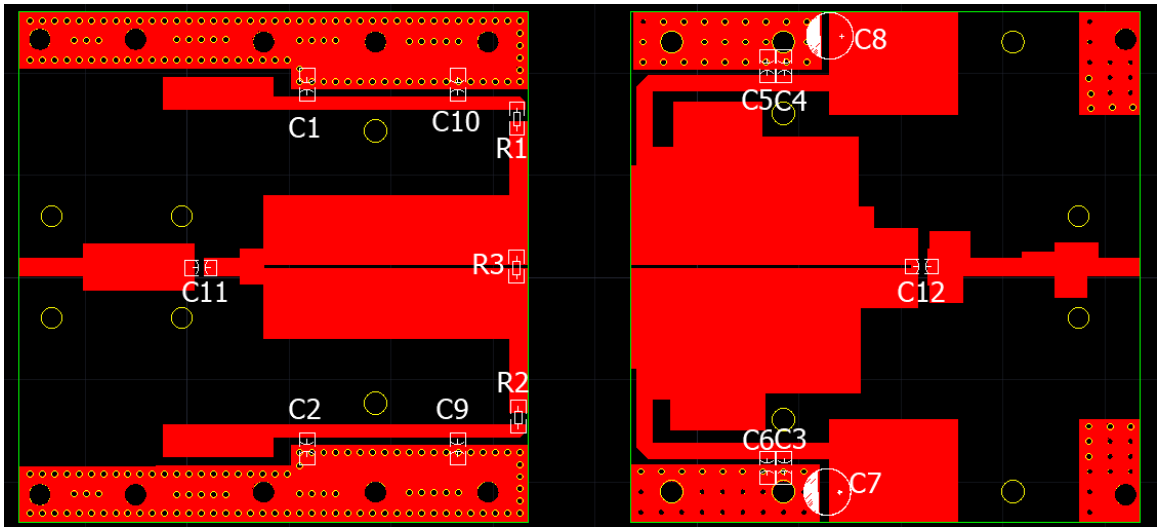


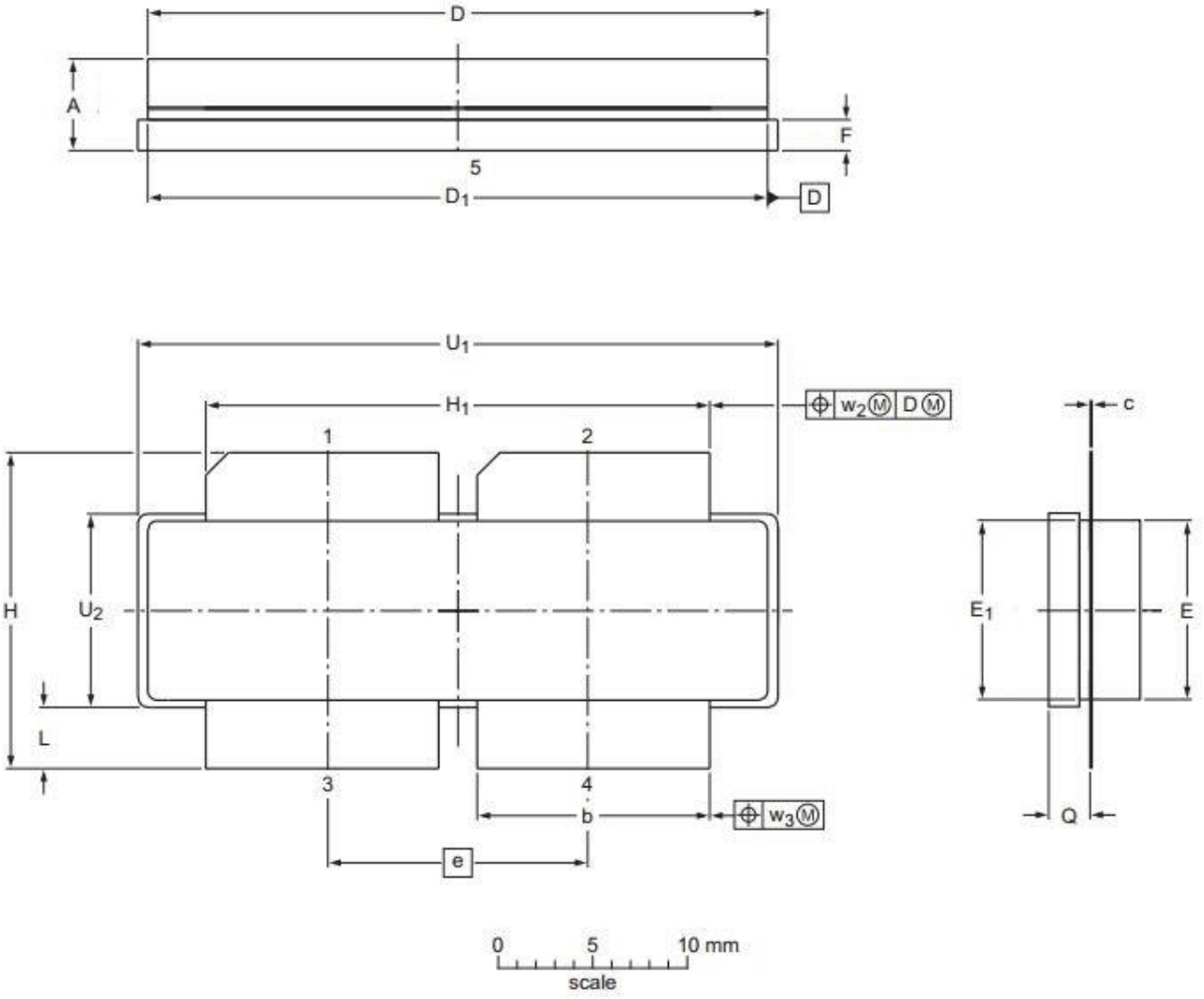
Figure 2: Reference design circuit (RO4350B, 30mil，PCB DWG file upon request,)



Component	Description	Suggestion
C1~C4	10uF/200V-1210	Ceramic multilayer capacitor
C5,C6,C9,C10	300pF	
C7,C8	4700uF/63V	Electrolytic Capacitor
C11	33pF	
C12	33pF	mica capacitor
R1,R2	18Ω-1206	Chip Resistor
R3	10Ω-2512	Chip Resistor

Package Outline

Earless flanged ceramic package; 4 leads（1、2—DRAIN、3、4—GATE、5—SOURCE）



UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	L	Q	U_1	U_2	W_2	W_2
mm	4.7 4.2	11.81 11.56	0.18 0.10	31.55 30.94	31.52 30.96	13.72	9.50 9.30	9.53 9.27	1.75 1.50	17.12 16.10	25.53 25.27	3.48 2.97	2.26 2.01	32.39 32.13	10.29 10.03	0.25	0.25
inches	0.185 0.165	0.465 0.455	0.007 0.004	1.242 1.218	1.241 1.219	0.540	0.374 0.366	0.375 0.365	0.069 0.059	0.674 0.634	1.005 0.995	0.137 0.117	0.089 0.079	1.275 1.265	0.405 0.395	0.01	0.01

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-D4					03/12/2013

Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2026/2/5	**V1.0**	**Preliminary Datasheet Creation, CV 17mm based**

Application data based on: TC-26-04

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