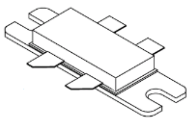
MK011K0UPX LDMOS TRANSISTOR

Document Number: MK011K0UPX
Preliminary Datasheet V1.1

800/1000W, 50V/60V High Power RF LDMOS FETs

MK011K0UPX



Description

The MK011K0UPX is a 50V 800W capable, highly rugged, unmatched LDMOS FET, designed for commercial and industrial applications with frequencies HF to 200MHz

At popular 50V,It could be the drop-in replacement of BLF184XR

It is featured for industry leading high power and high ruggedness, suitable for Industrial, Scientific and Medical application, as well as HF communication, VHF TV and Aerospace applications.

- Application data at multiple frequencies

Freq(MHz)	Voltage(V)/Idq(mA)	Signal type	Pin(dBm)	Pout(W)	Power Gain(dB)	Eff(%)
88	50/200	CW	41.5	820	17.5	80
1-100	50/200	CW	39-41.8	560-730	15.7-19.5	64-87
1-60	28/900	CW	37-39	310-420	16-19	70-80

Features

- High breakdown voltage enable possible class E operation at lower Vdd
- High Efficiency and Linear Gain Operations
- On chip RC network enable high stability and ruggedness
- Integrated ESD Protection
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Excellent thermal stability, low HCI drift
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain—Source Voltage	V_{DSS}	165	Vdc
Gate—Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case ,Case Temperature 85°C, 1100W CW, 50 Vdc, I_{DQ} = 240 Ma	$R_{\theta JC}$	0.18	°C/W
Transient thermal impedance from junction to case Tj = 150° C; tp = 100 us; Duty cycle = 20 %	Zth	0.026	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22—A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit

DC Characteristics

Drain-Source Voltage V_{GS}=0V, I_{DS}=1.0Ma	$V_{(BR)DSS}$		165		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50V, V_{GS} = 0 V)	I_{DSS}	———	———	1	μA
Gate—Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}	———	———	1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600 μA)	$V_{GS(th)}$	———	2.54	———	V
Gate Quiescent Voltage (V_{DD} = 50 V, I_D = 180 Ma, Measured in Functional Test)	$V_{GS(Q)}$	———	3.1	———	V
Drain source on state resistance (V_{DS} = 0.1V, V_{GS} = 10 V) Each section side of device measured	Rds(on)		190		mΩ
Common Source Input Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz) Each section side of device measured	C_{ISS}		600		Pf
Common Source Output Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz) Each section side of device measured	C_{OSS}		150		Pf
Common Source Feedback Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz) Each section side of device measured	C_{RSS}		4.5		Pf

88-108MHz

TYPICAL CHARACTERISTICS

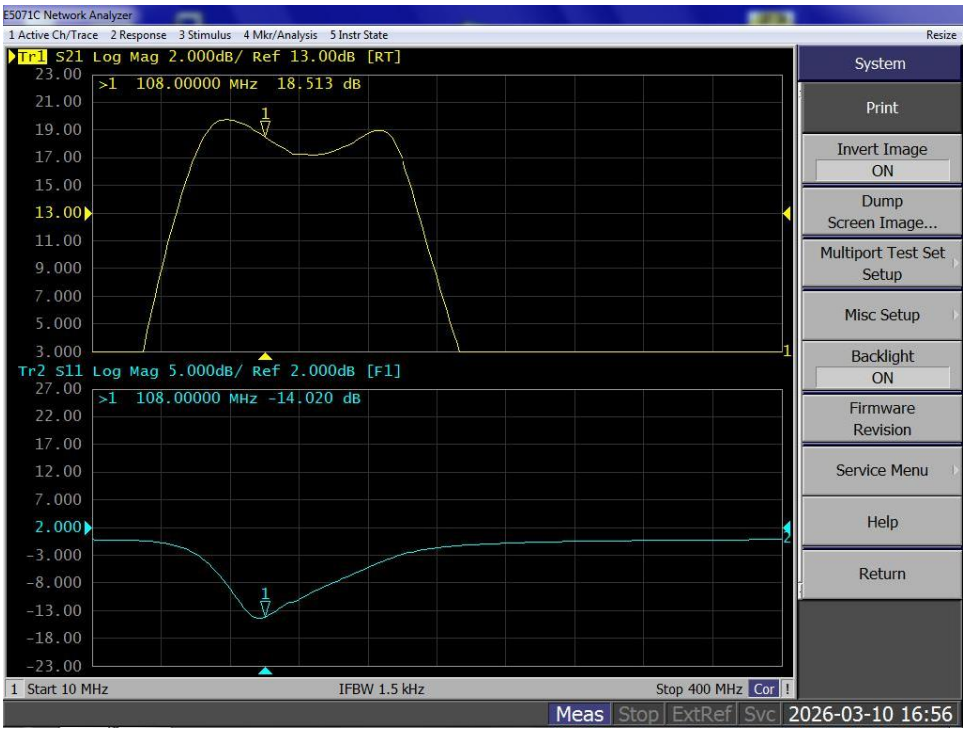


Figure 1: Network analyzer output S21/S11 (Vds=50V, Idq=1200mA)

Reference Circuit of Test Fixture (88-108MHz Power Amplifier)

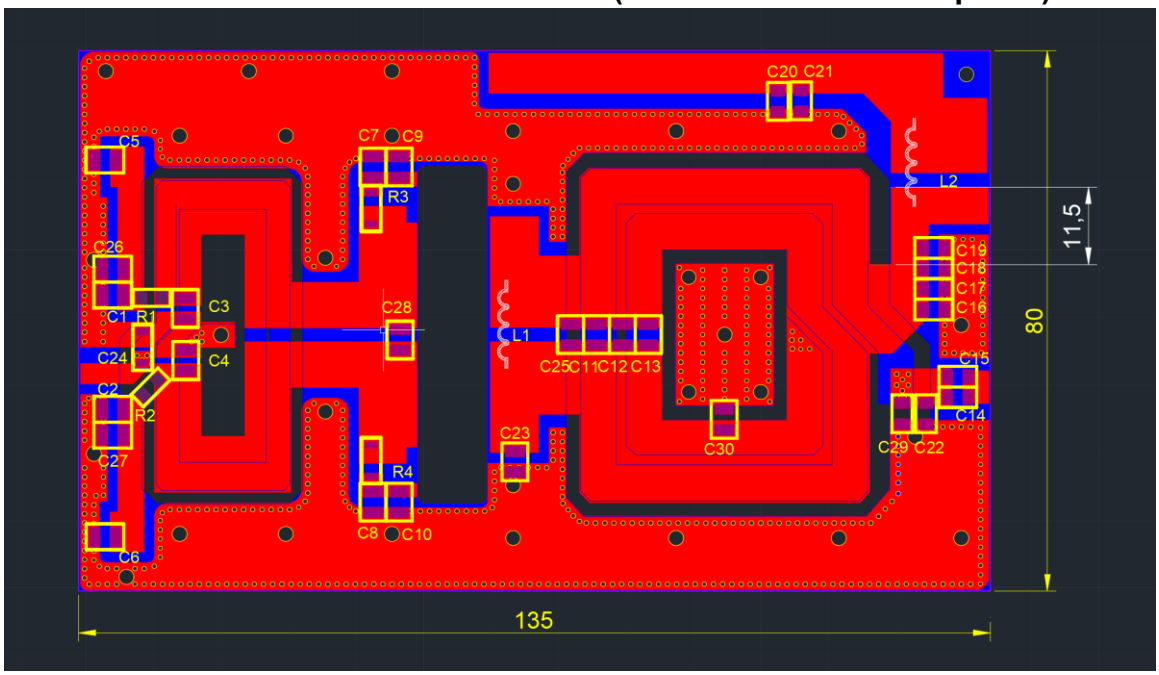


Table 5. Test Circuit Component Designations and Values

Component	Description	Suggested Manufacturer
C1~C4,C16~C18	560pF MQ301111	
C5,C6,C19~C22	10uF 1210	
C7,C8	910pF MQ301111	
C9,C10	470pF MQ301111	
C11	8.2pF MQ301111	
C12	15pF / 300V	
C13	33pF / 300V	
C14,C15	680pF / MQ101111	
R1,R2	360Ω 1206	/
R3,R4	51Ω 2512	/
L1	1.5mm wire ， 5mm inner diameter, 4Turns	DIY
L2	2.5mm wire ， 8mm inner diameter, 4Turns	DIY

1-100MHz

TYPICAL CHARACTERISTICS

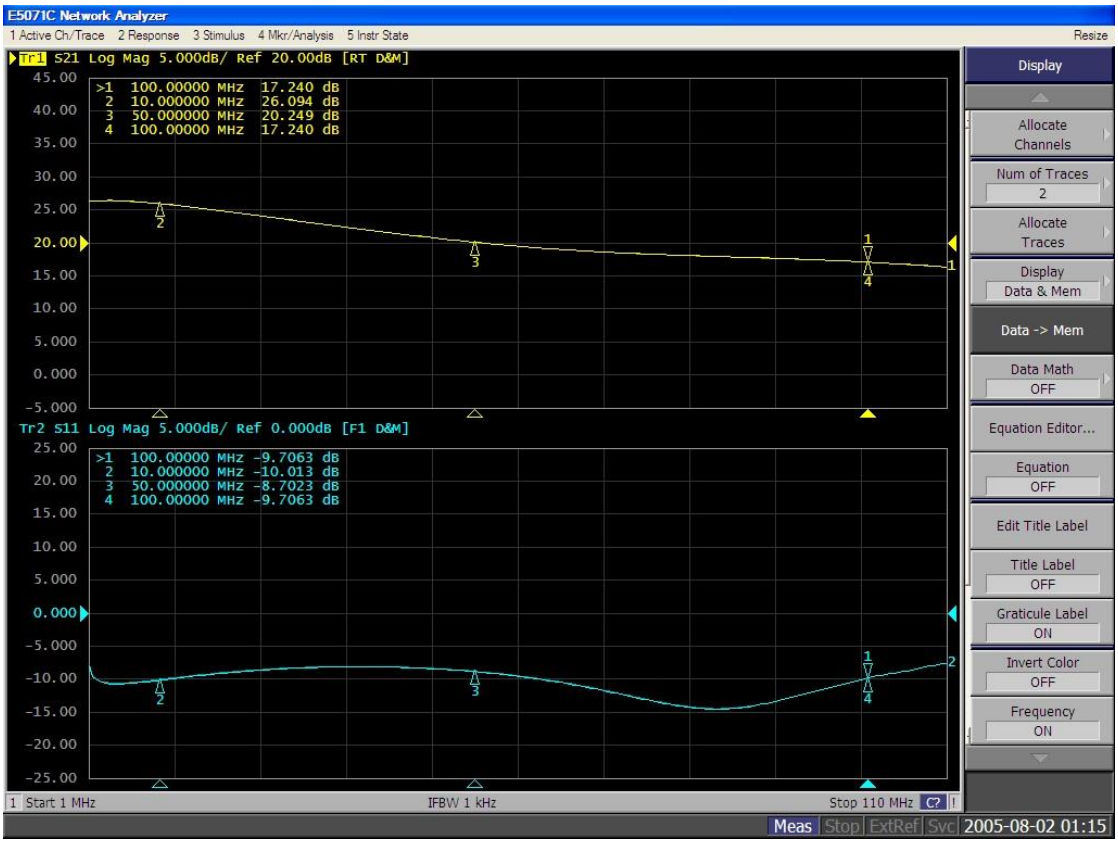
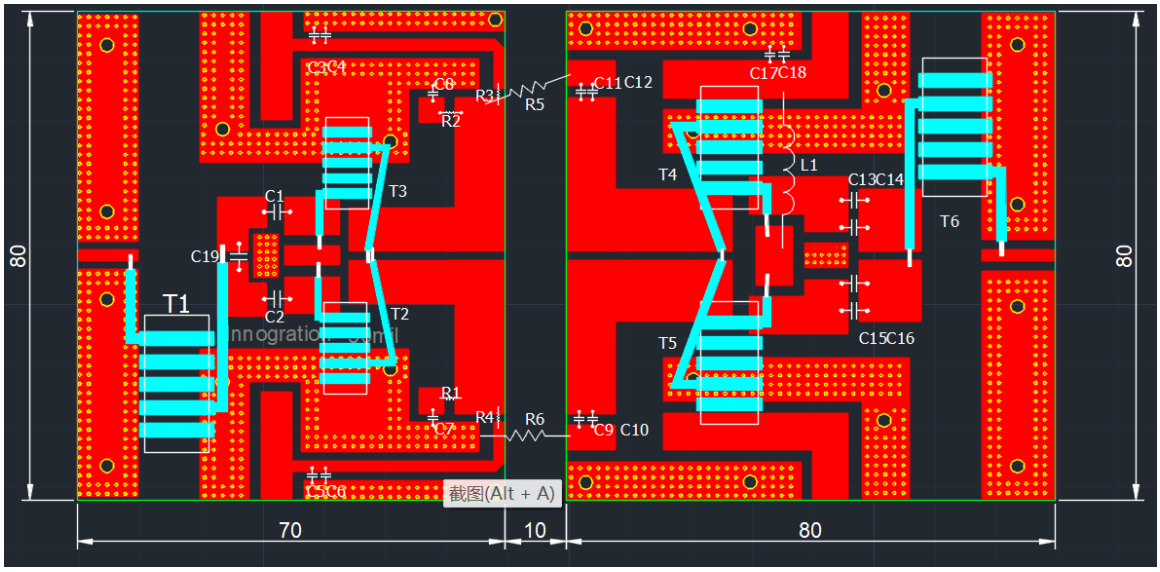


Figure 2: Network analyzer output S21/S11 (Vds=50V, Idq=1000mA)

Reference Circuit of Test Fixture



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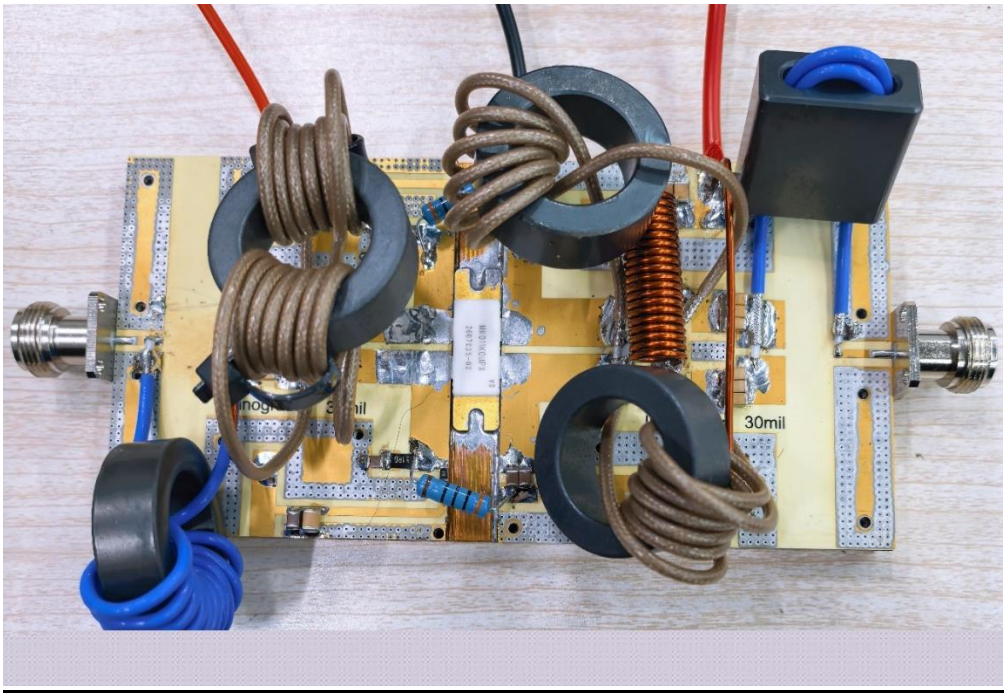
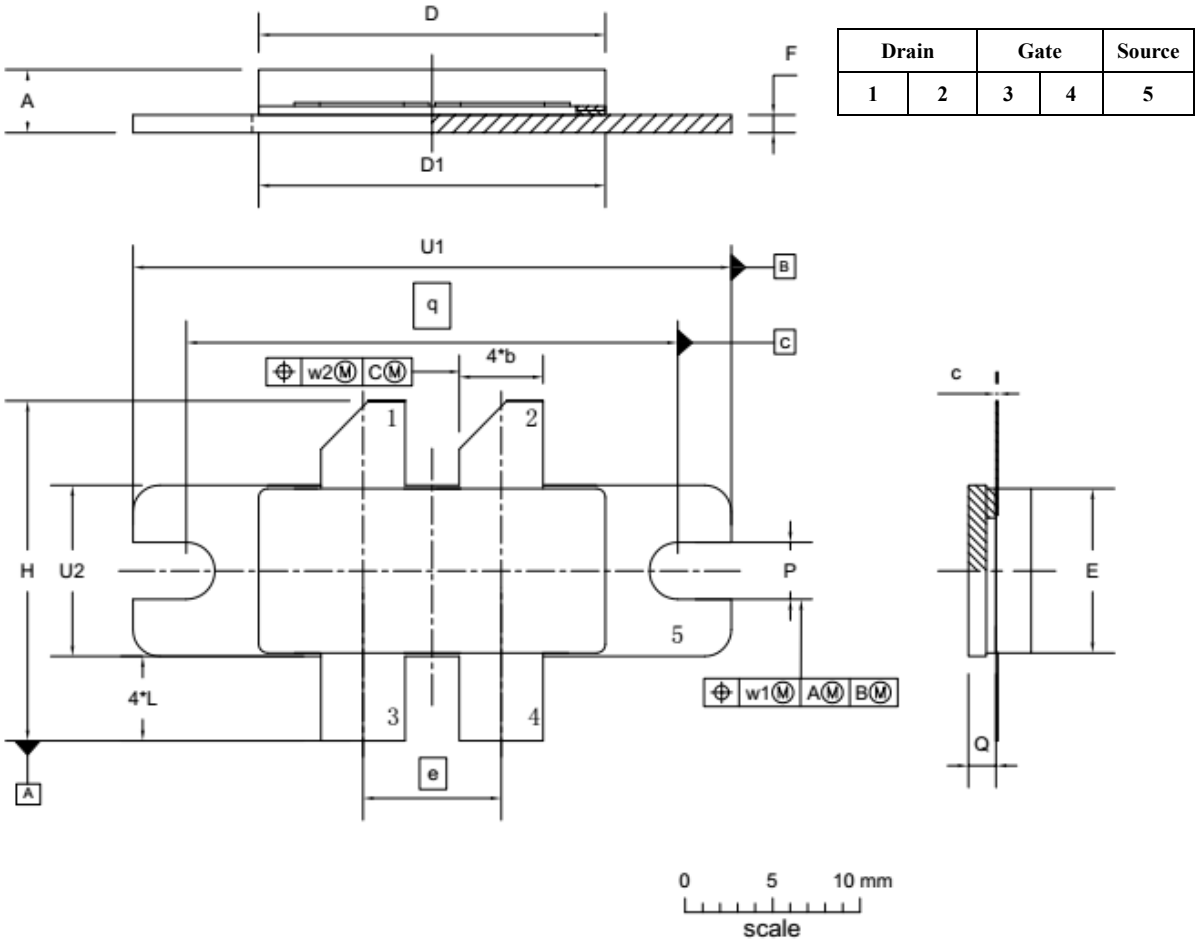


Table 6. Test Circuit Component Designations and Values

Component	Description	Suggestion
C3,C5,C7,C8,C9~C12,C18	10uF/1210	Ceramic Multilayer Capacitor
C1,C2,C4,C6,C13~C16 ,C17	2.2uF/1812	Ceramic Multilayer Capacitor
T1，T6	50ohm 500mm	SFRFBU-086-50,BN-43-7051
T2~T5	25ohm 500mm	SFF-25-1.5 FT-140-43
L1,L2	1.5mm wire ，8.0mm inner diameter, 20Turns	DIY
R3,R4	300Ω/1206	Pulg-in Resistor
R2,R1	50Ω/1206	Chip Resistor
R6,R5	300Ω/3W	TYT RFT-200
PCB	30Mil Rogers4350	

Package Outline

Eared Flanged Ceramic Package; 2 mounting holes; 4 leads



Drain		Gate		Source
1	2	3	4	5

UNIT	A	b	c	D	D_1	e	E	F	H	L	p	Q	q	U_1	U_2	W_1	W_2
mm	4.72 3.43	4.93 4.67	0.15 0.08	20.02 19.61	19.96 19.66	7.90	9.50 9.30	1.14 0.89	19.94 18.92	5.33 4.32	3.38 3.12	1.70 1.45	27.94	34.16 33.91	9.91 9.65	0.25	0.51
inches	0.186 0.135	0.194 0.184	0.006 0.003	0.788 0.772	0.786 0.774	0.311	0.374 0.366	0.045 0.035	0.785 0.745	0.210 0.170	0.133 0.123	0.067 0.057	1.100	1.345 1.335	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B4E					03/12/2013

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2026/3/5	Rev 1.0	Preliminary Datasheet
2026/4/24	Rev 1.1	Add 1-100M 500W data,1-60M 28V 300W data

Application data based on SYX-26-12/26-18， TC-26-14

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