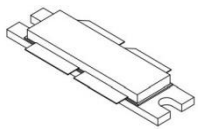
MQ1042VP LDMOS TRANSISTOR

Document Number: MQ1042VP
Preliminary Datasheet V1.0

400W, UHF band 50V High Power RF LDMOS FETs

MQ1042VP



Description

The MQ1042VP is a 400W capable, Input/Output matched LDMOS FET, designed for commercial and industrial applications within UHF band up to 1GHz, supporting both pulse and CW applications, **as the bandwidth extension and performance enhancement of MX1040VP within UHF band**

There isn't guarantee when this device is used outside of the band stated above.

- Typical RF performance within 470-900MHz , with device soldered

MQ1042VP[V1] VGS=3.3V VDS=50V IDQ=150mA pulse 100us 10%								
Freq (MHz)	Psat (dBm)	Psat (W)	IDS (A)	Pin (dBm)	Gain (dB)	Eff(%)	2nd （dBc）	3rd （dBc）
460	56.59	456.0	1.54	43.60	12.99	64.69	-25.70	-14.80
470	57.12	515.2	1.72	42.40	14.72	64.81	-27.20	-18.50
500	56.57	453.9	1.42	43.70	12.87	70.38	-23.10	-21.30
550	56.92	492.0	1.54	42.74	14.18	69.79	-25.00	-26.10
600	56.85	484.2	1.66	42.10	14.75	63.29	-26.40	-26.60
650	56.60	457.1	1.65	42.85	13.75	60.14	-27.10	-33.00
700	56.94	494.3	1.80	42.10	14.84	59.20	-27.00	-33.70
750	57.11	514.0	1.91	42.31	14.80	57.76	-29.90	-34.80
800	57.40	549.5	2.06	43.15	14.25	56.95	-29.80	-26.80
850	57.46	557.2	2.10	43.78	13.68	56.57	-25.70	-37.30
900	56.77	475.3	1.59	42.59	14.18	65.11	-27.80	-47.50
910	56.35	431.5	1.44	43.13	13.22	65.88	-35.40	-49.00

Features

- High breakdown voltage enable high ruggedness
- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Excellent thermal stability, low HCI drift
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	110	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case ,Case Temperature	$R_{\theta JC}$	0.22	°C/W

25°C, 400 CW, 50Vdc, I_{DQ} = 150 mA			

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage V_{GS}=0V, I_{DS}=1.0mA	$V_{(BR)DSS}$		110		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate—Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600 μA)	$V_{GS}(th)$	——	2.54	——	V
Gate Quiescent Voltage (V_{DD} = 50 V, I_D = 150 mA, Measured in Functional Test)	$V_{GS(Q)}$	——	3.3	——	V

470-900MHz

TYPICAL CHARACTERISTICS

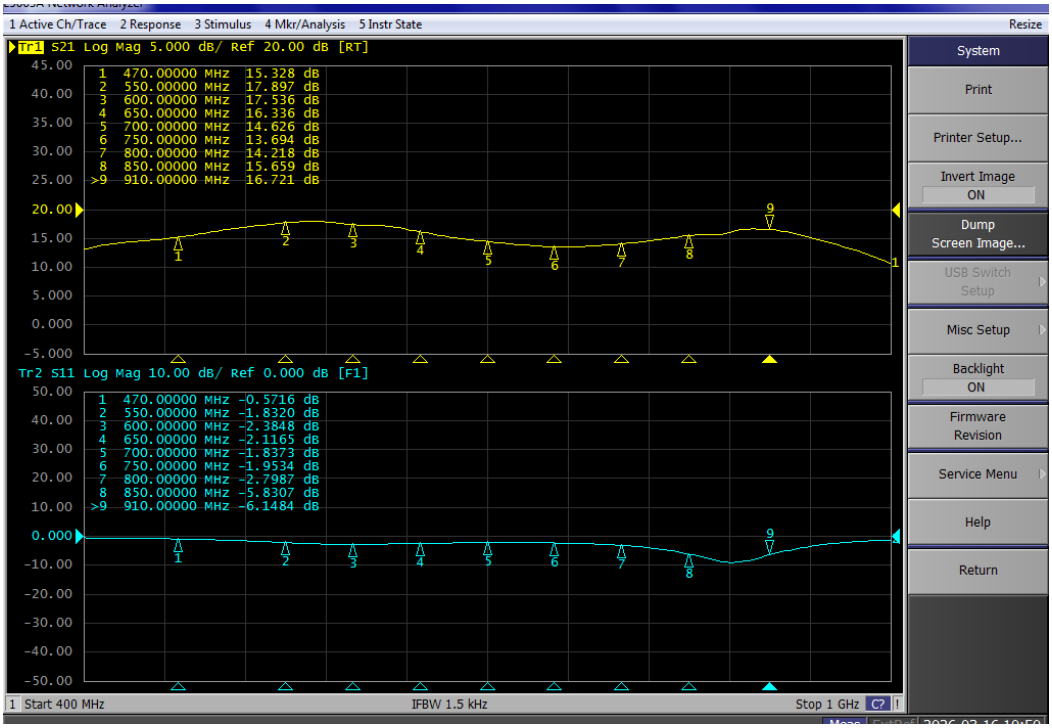
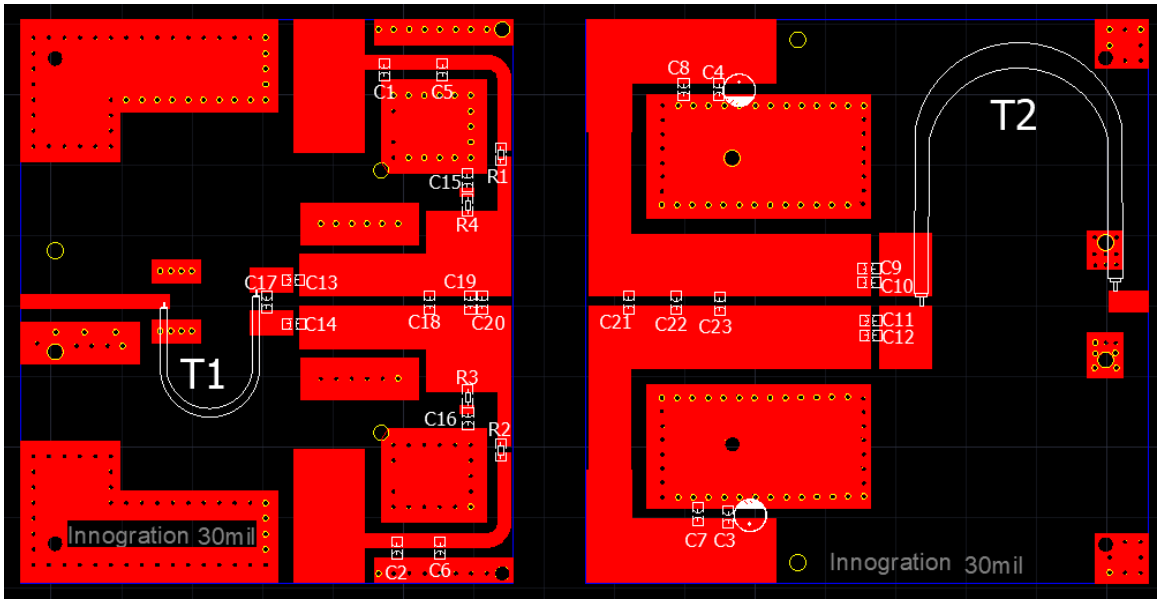


Figure 1: Network analyzer output, S11 (Vds=50V,Idq=1A)

Reference Circuit of Test Fixture

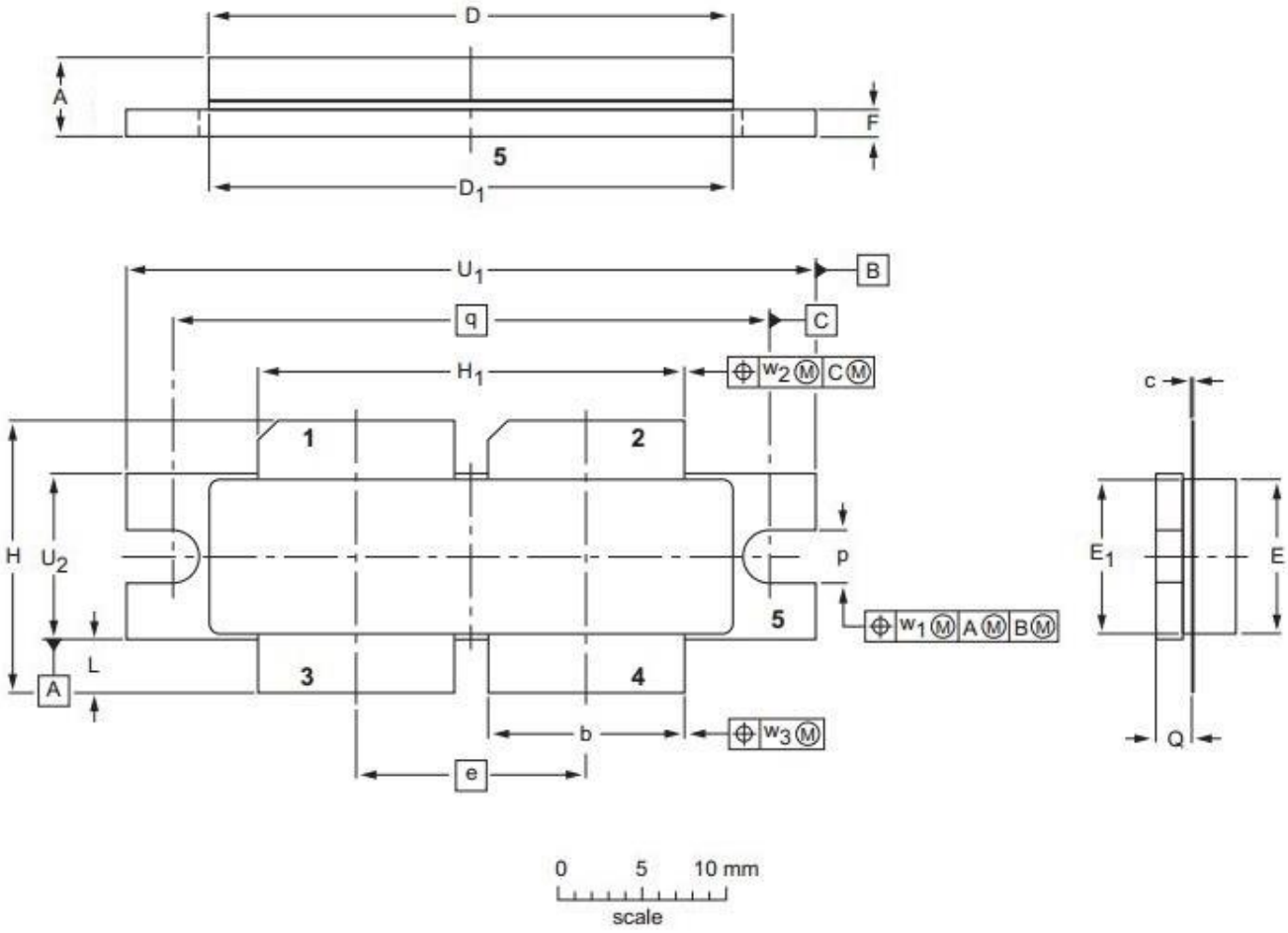
(Layout file upon request) PCB: Roger 4350B, 30mils



Component	Description	Suggestion
C1~C4,C15,C16	10uF/200V-1210	Ceramic multilayer capacitor
C5~C8	470pF	
C9~C12	47pF	
C13,C14	27pF	
C17	2pF	
C18	6.8pF	
C19	9.1pF	
C20	3.3pF	
C21	2.2pF	
C22	5.6pF	
C23	3.6pF	
R1,R2	100Ω/1206	Chip Resistor
R3,R4	10Ω/1206	Chip Resistor
T1	25ohm-60mm	RFSFBU-086-25
T2	35ohm-70mm	SFF-35-3

Package Outline

Flanged ceramic package; 2 mounting holes; 4 leads（1、2—DRAIN、3、4—GATE、5—SOURCE）



UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	L	p	Q	q	U_1	U_2	W_1	W_2	W_2
mm	4.7 4.2	11.81 11.56	0.18 0.10	31.55 30.94	31.52 30.96	13.72	9.50 9.30	9.53 9.27	1.75 1.50	17.12 16.10	25.53 25.27	3.48 2.97	3.30 3.05	2.26 2.01	35.56	41.28 41.02	10.29 10.03	0.25	0.51	0.25
inches	0.185 0.165	0.465 0.455	0.007 0.004	1.242 1.218	1.241 1.219	0.540	0.374 0.366	0.375 0.365	0.069 0.059	0.674 0.634	1.005 0.995	0.137 0.117	0.130 0.120	0.089 0.079	1.400	1.625 1.615	0.405 0.395	0.01	0.02	0.01

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-D4E					03/12/2013

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2026/3/16	Rev 1.0	Preliminary Datasheet

Application data based on TC-26-07

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