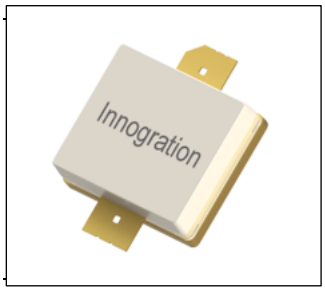
ITJV01500A2C LDMOS TRANSISTOR

Document Number: ITJV01500A2C
Advanced Datasheet V1.0

300W/500W, 50/65V High Power RF LDMOS FETs



Description

The ITEV01500A2C is a 50V 300-watt capable, high performance, highly rugged，unmatched，single ended LDMOS FET, designed for commercial and industrial applications with frequencies HF to 200MHz, in new generation highly cost effective open cavity package.
It is featured by single ended configuration for high power and high ruggedness, suitable for Industrial, Scientific and Medical application

- Typical performance(on Innogration test board with device soldered)
  Signal: CW , Vgs=3.45V,Vds=50V,Idq=200mA

Freq (MHz)	Pin (dBm)	Pout (dBm)	Pout (W)	Ids (A)	Gain (dB)	Eff (%)	2nd harmonic (dBc)
40.68	35	55	320	8.1	20	80	-25

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large PosITJVe and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 136-174MHz (Commercial ground communication)
- Laser Exciter
- Synchrotron
- MRI
- Plasma generator
- Weather Radar

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+185	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+65	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	RθJC	0.35	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (T_A = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics (per half section)					
Drain-Source Voltage V_{GS}=0, I_{DS}=1.0mA	$V_{(BR)DSS}$		185		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 75V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50 V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate--Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600 μA)	$V_{GS}(th)$	——	2.65	——	V
Gate Quiescent Voltage (V_{DD} = 50 V, I_D = 200 mA, Measured in Functional Test)	$V_{GS(Q)}$	——	3.4	——	V

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 50 Vdc, I_{DQ} = 100 mA, f =100MHz, pulse width:100us, duty cycle:10%

Load 65:1 All phase angles, at 300W Pulsed CW Output Power	No Device Degradation

40.68MHz

TYPICAL CHARACTERISTICS

Figure 1: CW Gain and Power Efficiency as a Function of Pout at 40.68MHz

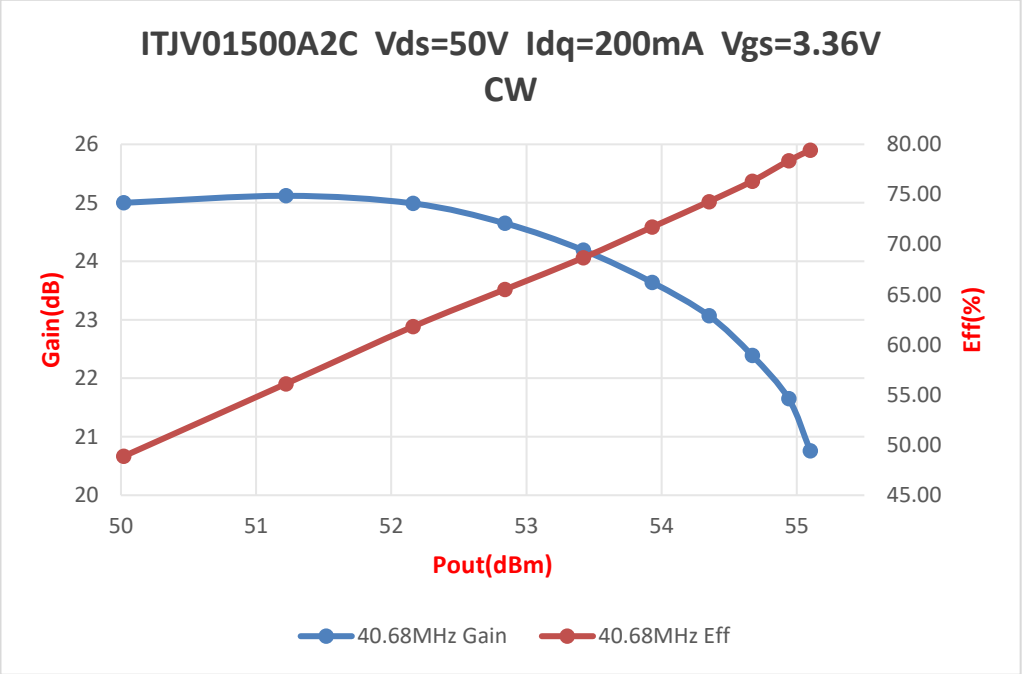
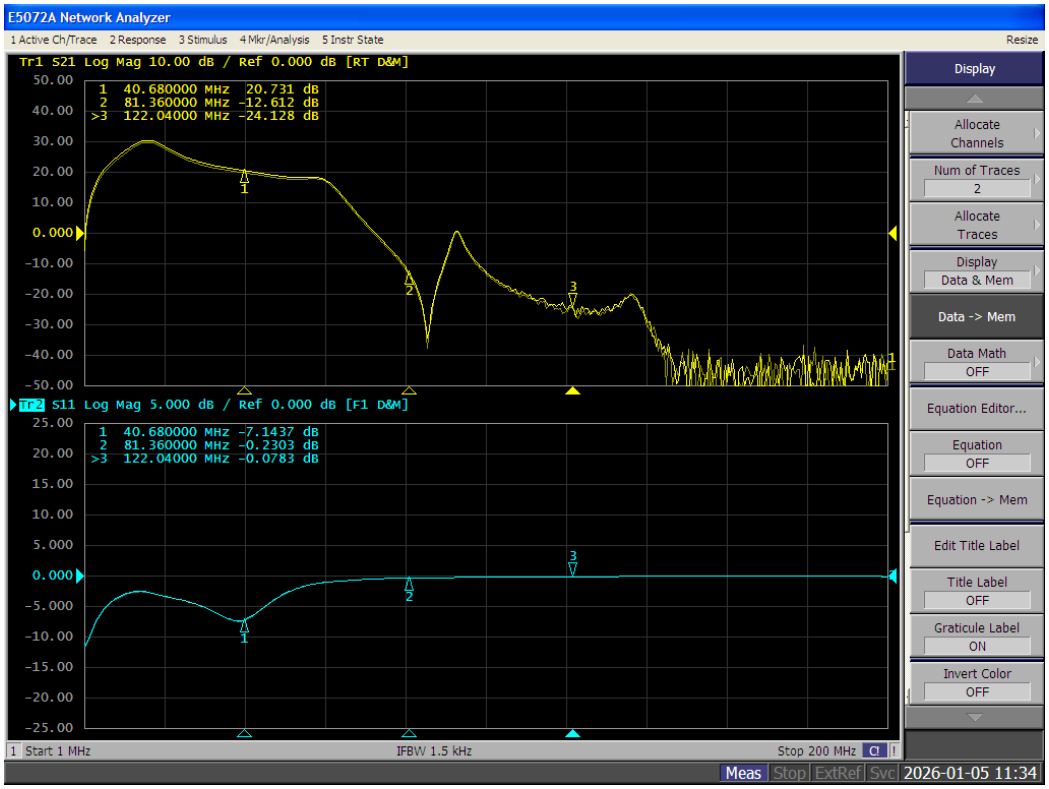


Figure 2: Network analyzer output S11/S21



Reference Circuit of Test Fixture Assembly Diagram

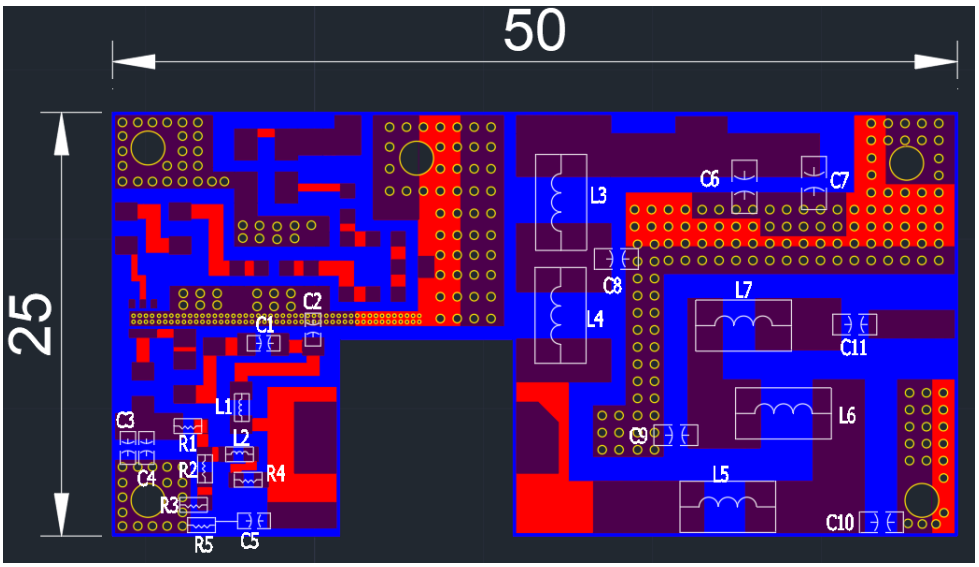
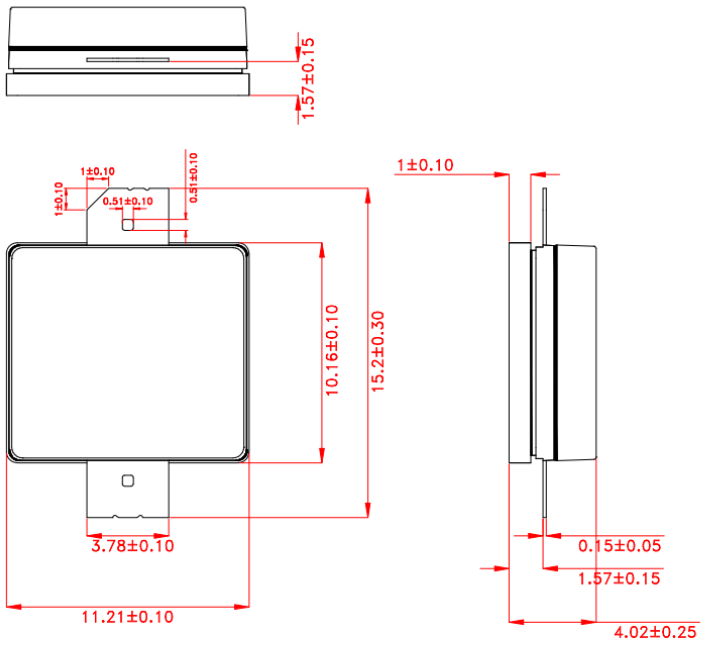
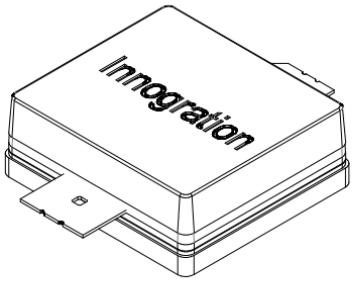


Table 5. Test Circuit Component Designations and Values

C1,C4	10nF/0805	/
C2	120pF/MQ301111	
C3	1uF/0805	
C5,C7	10uF/1210	
C6,C11	1000pF/MQ301111	
C8	82pF/MQ301111	
C9	200pF/MQ301111	
C10	75pF/MQ301111	
R1	3000Ω/0603	
R2	6200Ω/0603	
R3	0.1Ω/0603	
R4	220Ω/0805	
R5	51Ω/0805	
L1	120nH/0805	
L2	82nH/0805	
L3,L4	2mm wire，6 turns, Φ=5mm	DIY
L5	2mm wire，3 turns, Φ=5mm	DIY
L6	2mm wire，4 turns, Φ=5mm	DIY
L7	2mm wire，3 turns, Φ=5mm	DIY

Package Dimensions （Unit:mm）





Unit:mm

Tolerance ±0.10mm,Except as Noted.

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2026/1/5	Rev 1.0	Advanced Datasheet Creation

Application data based on SJJ-26-01

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