



## GaN HEMT 50V, 650W, 1.8-2.2GHz Full band RF Power Transistor

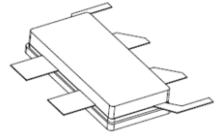
### Description

The STCV22W650BY4V is a dual path 650watt, Internally matched GaN HEMT, ideal for applications from 1.8 to 2.2GHz full band operation especially for LTE/5G

There is no guarantee of performance when this part is used outside of stated frequencies.

- Typical RF performance on **1.8-2.2GHz** full band asymmetrical Doherty with device soldered VDS= 50V, IDQ=200mA(Vgm=-3.05V, Vgp=-5.5V)

**STCV22W650BY4V**



Freq (GHz)	Pulse CW Signal <sup>(1)</sup>				P <sub>avg</sub> =49.5dBm WCDMA Signal <sup>(2)</sup>		
	P3 (dBm)	P3 (W)	P4 (dBm)	P4 (W)	Gp (dB)	η <sub>D</sub> (%)	ACPR <sub>5M</sub> (dBc)
1.80	57.18	522.9	58.1	645.0	14.0	55.5	-23.1
1.85	56.04	401.8	58.26	669.6	13.9	57.2	-23.6
1.90	55.76	376.8	58.29	675.0	13.9	57.3	-23.8
2.00	56.83	482.4	58.20	660.6	14.2	56.7	-26.1
2.11	58.02	633.7	58.5	707.6	14.6	56.0	-26.8
2.15	57.98	628.3	58.32	679.2	14.9	55.7	-27.4
2.175	57.83	606.8	58.12	649.2	14.8	55.7	-27.0

(1) Pulsed condition: 100us and 10%,

(2) 1C WCDMA; Signal PAR = 10 dB @ 0.01% Probability on CCDF.

### Applications

- Asymmetrical Doherty amplifier within 1.8-2.2GHz full band
- Sub-2GHz power amplifier
- CW or pulsed Amplifier

### Important Note: Proper Biasing Sequence for GaN HEMT Transistors

#### Turning the device ON

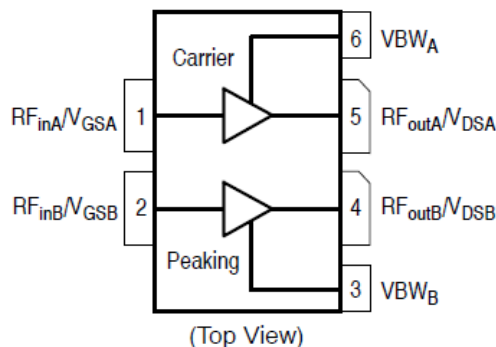
1. Set VGS to the pinch-off (VP) voltage, typically -5 V
2. Turn on VDS to nominal supply voltage
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

#### Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically -5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

Figure 1: Pin Connection definition

Transparent top view (Backside grounding for source)





**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain--Source Voltage	$V_{DSS}$	+200	Vdc
Gate--Source Voltage	$V_{GS}$	-8 to +0.5	Vdc
Operating Voltage	$V_{DD}$	55	Vdc
Maximum gate current	$I_{gs}$	83	mA
Storage Temperature Range	$T_{stg}$	-65 to +150	°C
Case Operating Temperature	$T_C$	+150	°C
Operating Junction Temperature	$T_J$	+225	°C

**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case by FEA $T_C= 85^\circ\text{C}$ , at $P_d=90\text{W}$ , on Doherty application board	$R_{\theta JC}$	0.85	°C /W

**Table 3. Electrical Characteristics (TA = 25°C unless otherwise noted)**

**DC Characteristics ( Main path, measured on wafer prior to packaging)**

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS}=-8\text{V}$ ; $I_{DS}=30\text{mA}$	$V_{DSS}$		200		V
Gate Threshold Voltage	$V_{DS}=10\text{V}$ , $I_D=3\text{mA}$	$V_{GS(th)}$	-4		-2	V
Gate Quiescent Voltage	$V_{DS}=50\text{V}$ , $I_{DS}=300\text{mA}$ , Measured in Functional Test	$V_{GS(Q)}$		-3.1		V

**DC Characteristics ( Peak path, measured on wafer prior to packaging)**

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS}=-8\text{V}$ ; $I_{DS}=56\text{mA}$	$V_{DSS}$		200		V
Gate Threshold Voltage	$V_{DS}=10\text{V}$ , $I_D=56\text{mA}$	$V_{GS(th)}$	-4		-2	V
Gate Quiescent Voltage	$V_{DS}=50\text{V}$ , $I_{DS}=500\text{mA}$ , Measured in Functional Test	$V_{GS(Q)}$		-3.1		V

**Ruggedness Characteristics**

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Load mismatch capability	2.14GHz, $P_{out}=90\text{W}$ WCDMA 1 Carrier in Doherty circuit All phase, No device damages	VSWR		10:1		

**Figure 2: Median Lifetime vs. Channel Temperature**

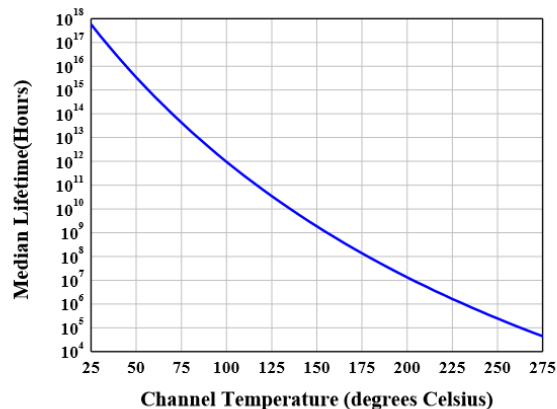




Figure 3: Efficiency and power gain as function of Pout (1.8-2.2GHz Doherty)

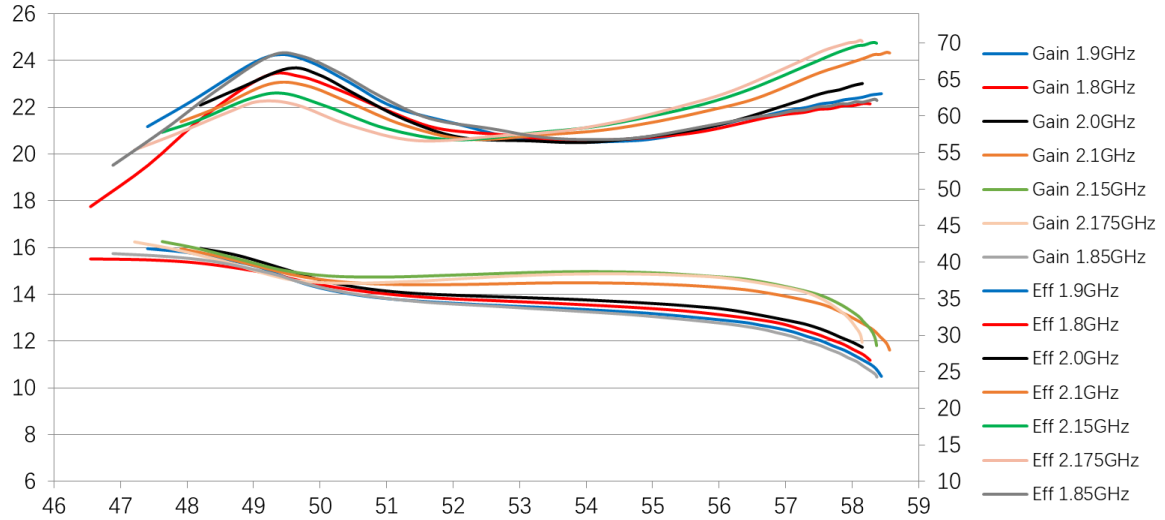
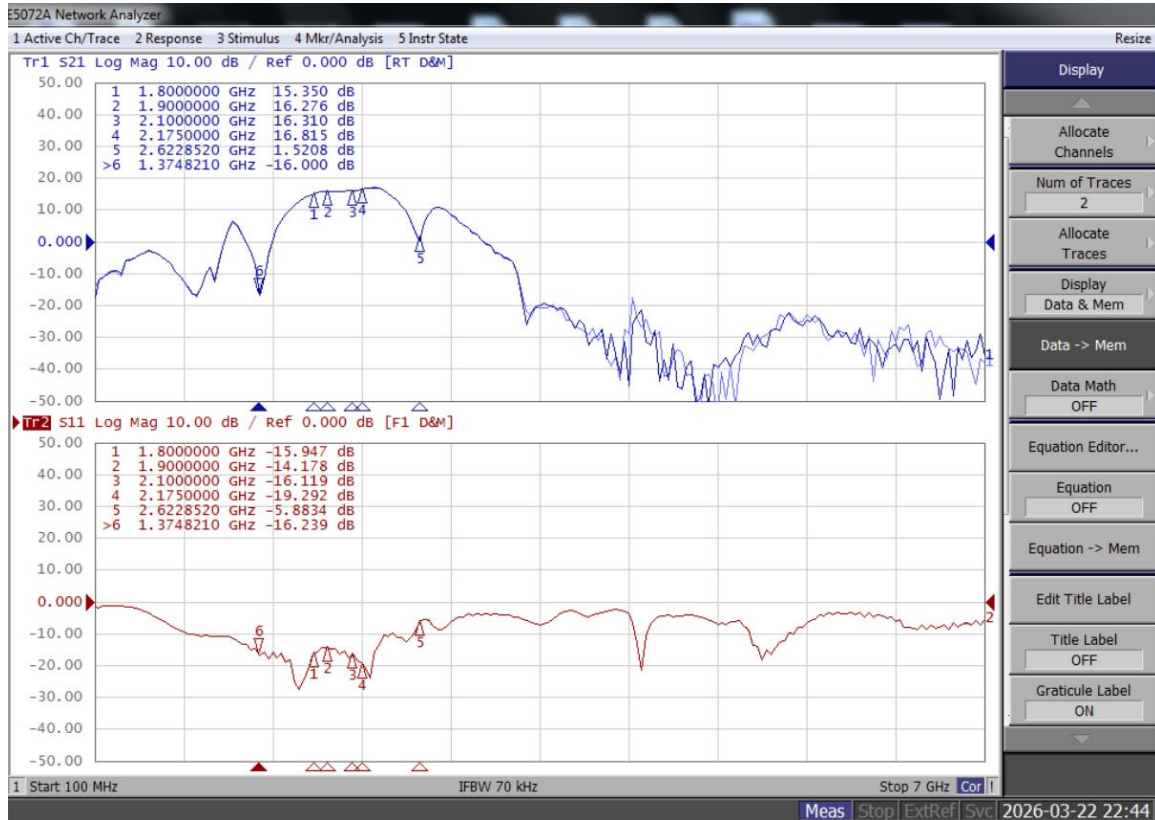
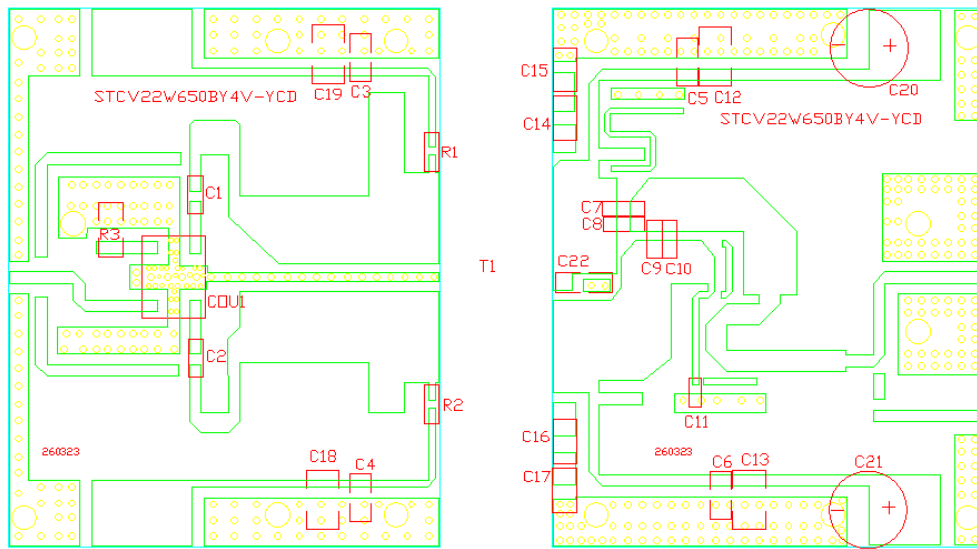


Figure 4: Network analyzer output, S11 and S21 (1.8-2.2GHz Doherty)



**Figure 5: Picture of application board Doherty circuit for 1.8-2.2GHz**

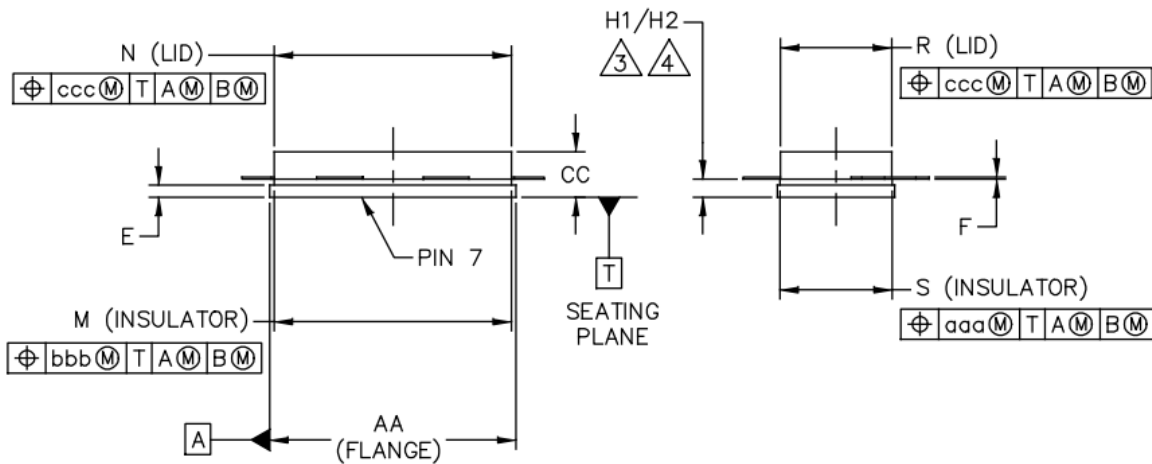
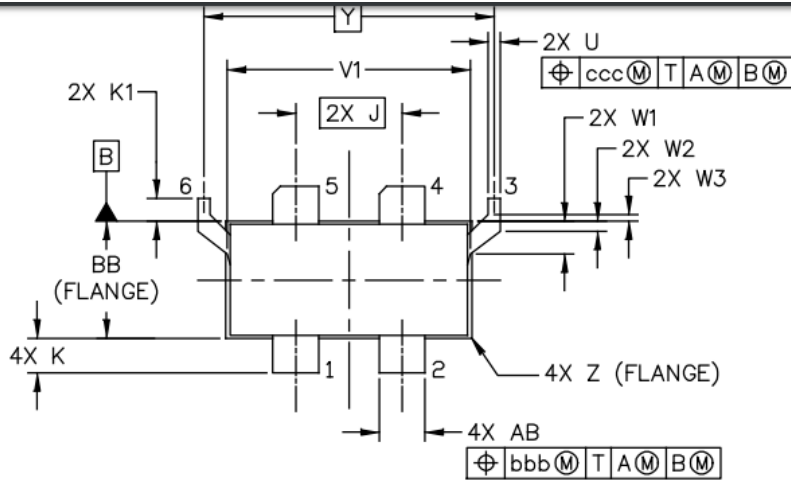


**Table 4. Bill of materials of application board (PCB layout upon request, RO4350B 20mils)**

Part	Quantity	Description	Part Number	Manufacture
C1,C2,C3,C4 C5,C6,C11	7	20pF High Q Capacitor	251SHS200BSE	TEMEX
C22	1	1.1pF High Q Capacitor	251SHS1R1BSE	TEMEX
C7,C8	2	6.2pF High Q Capacitor	251SHS6R2BSE	TEMEX
C9,C10	2	3.9pF High Q Capacitor	251SHF3R9BSE	TEMEX
C18,C19	2	4.7nF		
C20,C21	2	470uF		
C12,C13,C14,C15,C16,C17	6	10uF MLCC	GRM32EC72A106ME05	Murata
C5	1	10pF High Q Capacitor	251SHS100BSE	TEMEX
R1,R2	2	10 $\Omega$ Power Resistor	ESR03EZPF100	ROHM
R3	1	50 $\Omega$ Power Resistor	RFR50-20CT0421B	YT
COU1	1	3 dB Bridge	HC2100P03H	YANTEL
T1	1	650W GaN Dual Transistor	STCV22W650BY4V	Innogrations



Earless Flanged Ceramic Package; 6 leads- BY4V



DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
AA	.805	.815	20.45	20.70	R	.365	.375	9.27	9.53
BB	.380	.390	9.65	9.91	S	.365	.375	9.27	9.53
CC	.125	.170	3.18	4.32	U	.035	.045	0.89	1.14
E	.035	.045	0.89	1.14	V1	.795	.805	20.19	20.45
F	.004	.007	0.10	0.18	W1	.0975	.1175	2.48	2.98
H1	.057	.067	1.45	1.70	W2	.0225	.0425	0.57	1.08
H2	.054	.070	1.37	1.78	W3	.0125	.0325	0.32	0.83
J	.350 BSC		8.89 BSC		Y	.956 BSC		24.28 BSC	
K	.0995	.1295	2.53	3.29	Z	R.000	R.040	R0.00	R1.02
K1	.070	.090	1.78	2.29	AB	.145	.155	3.68	3.94
M	.774	.786	19.66	19.96	aaa	.005		0.13	
N	.772	.788	19.61	20.02	bbb	.010		0.25	
					ccc	.015		0.38	



## Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2024/3/13	V1.0	Preliminary Datasheet Creation
2024/4/3	V1.1	Application optimization
2026/3/24	V2.0	Application optimization on main path

Application data based on: LWH-24-10/12/26-08

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