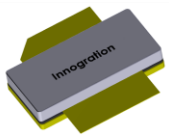
S3K071K2RVS GaN TRANSISTOR

Document Number: S3K071K2RVS
Preliminary Datasheet V1.0

GaN 50V 1200W, RF Power Transistor

S3K071K2RVS



Description

The S3K071K2RVS is a 1200W single ended GaN HEMT, designed for multiple applications with frequencies up to 700MHz. **It offers much smaller and simpler matching circuit than traditional push-pull matching circuit ,as key benefit to customers.**

It is recommended to use this part for pulsed CW application only.

There is no guarantee of performance when this part is used in applications designed Outside of these frequencies.

- Typical performance (on Innogration narrow band production fixture with device soldered)

V_{DS}= 50V, I_{DQ}=300mA(V_{GS}=-3.15V), 100us,10%

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
423	60.51	1124.6	64.7	19.43	61.21	1321.8	67.7
433	60.30	1072.6	72.0	19.20	60.99	1255.0	76.4
443	59.49	888.4	72.3	18.66	60.05	1011.8	75.2

Applications and Features

- Suitable for wireless communication infrastructure, wideband amplifier, EMC testing, ISM etc.
- High Efficiency and Linear Gain Operations
- Thermally Enhanced Industry Standard Package
- High Reliability Metallization Process
- Excellent thermal Stability and Excellent Ruggedness
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

Turning the device ON

1. Set VGS to the pinch--off (VP) voltage, typically –5 V
2. Turn on VDS to nominal supply voltage (50V)
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically –5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+150	Vdc
Gate--Source Voltage	V_{GS}	-8 to 0	Vdc
Operating Voltage	V_{DD}	0 to 55	Vdc
Maximum forward gate current	Igf	54	mA
Storage Temperature Range	Tstg	-65 to +150	C
Case Operating Temperature	T_C	-55 to +150	C
Operating Junction Temperature	T_J	+225	C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, DC Power Dissipation, FEA	$R_{\theta JC}$	0.25	C/W

Table 3. Electrical Characteristics (T_C = 25℃ unless otherwise noted)

DC Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V_{GS}=-8V; I_{DS}=162mA	V_{DSS}		150		V
Gate Threshold Voltage	V_{DS} = 50V, I_D = 162mA	V_{GS}(th)		-3.4		V
Gate Quiescent Voltage	V_{DS} =50V, I_{DS}=300mA, Measured in Functional Test	$V_{GS(Q)}$		-3.15		V

433MHz

Reference Circuit of Test Fixture Assembly Diagram

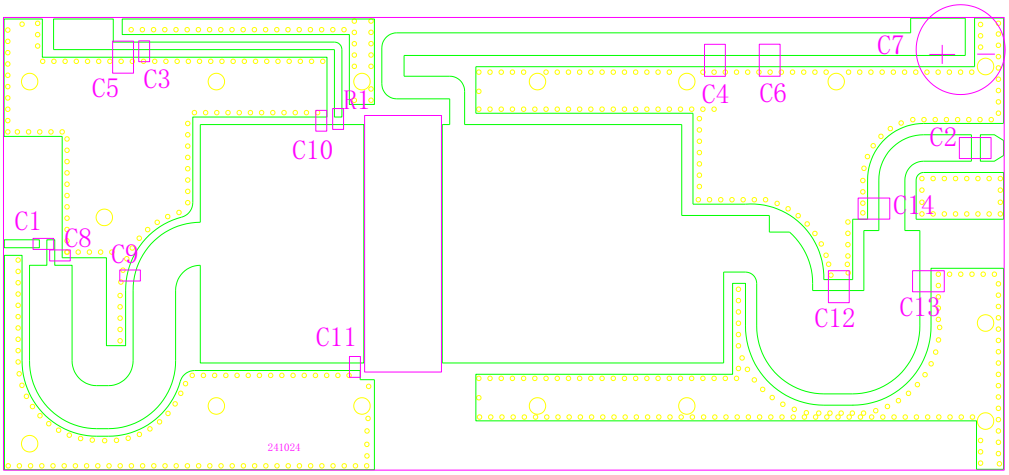


Figure 1. Test Circuit Component Layout (425-475MHz) RO4350B 20mils

Table 4. Test Circuit Component Designations and Values

Designator	Footprint	Comment	Quantity
C1, C8	0603/0805	10 pF	2
C2, C4	1210	100 pF	2
C3	0603/0805	100 pF	1
C5, C6	1210	10uF/100V	2
C7		1000uF/63V	1
C9	0603/0805	20 pF	5
C10, C11	0603/0805	30 pF	2
C12	1210	3 pF	1
C13, C14	1210	10 pF	2
R1	0603/0805	10Ω	1

Figure 2. Network Analyzer result S11 and S21 Vgs = -3.1V, VDS= 50V, IDQ = 1000mA

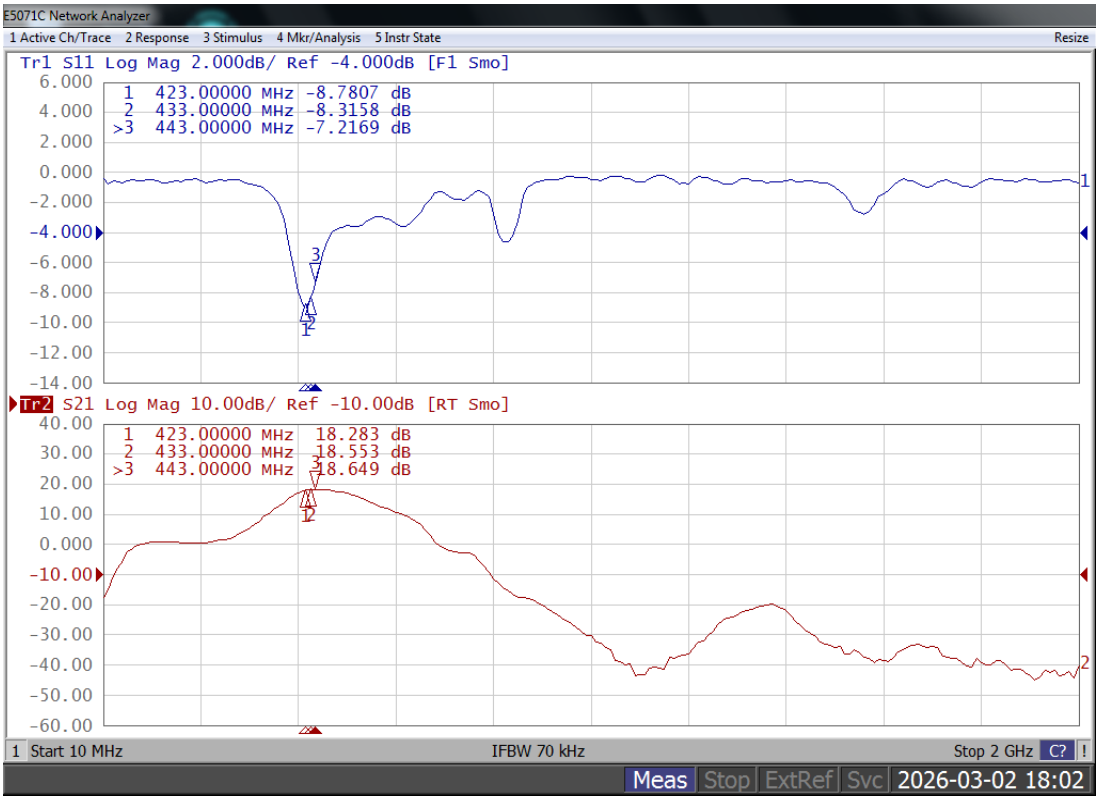
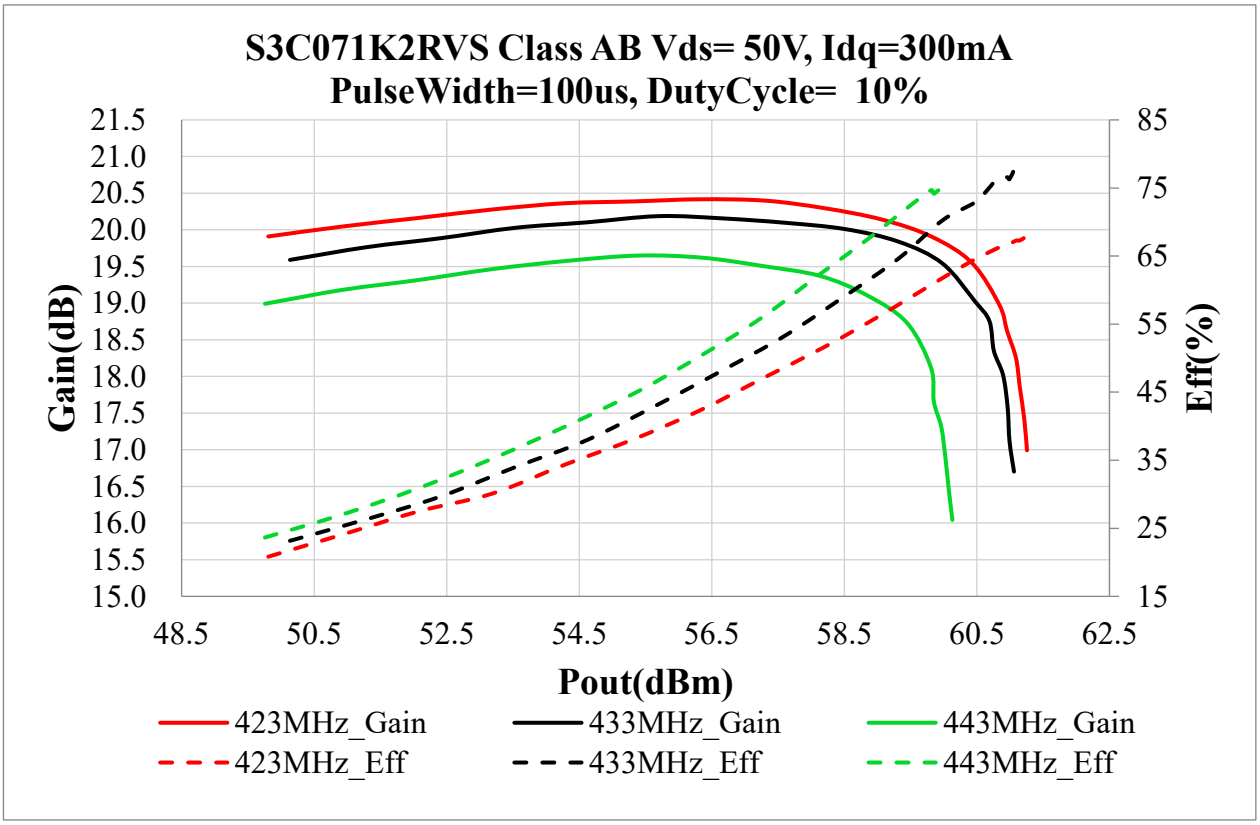
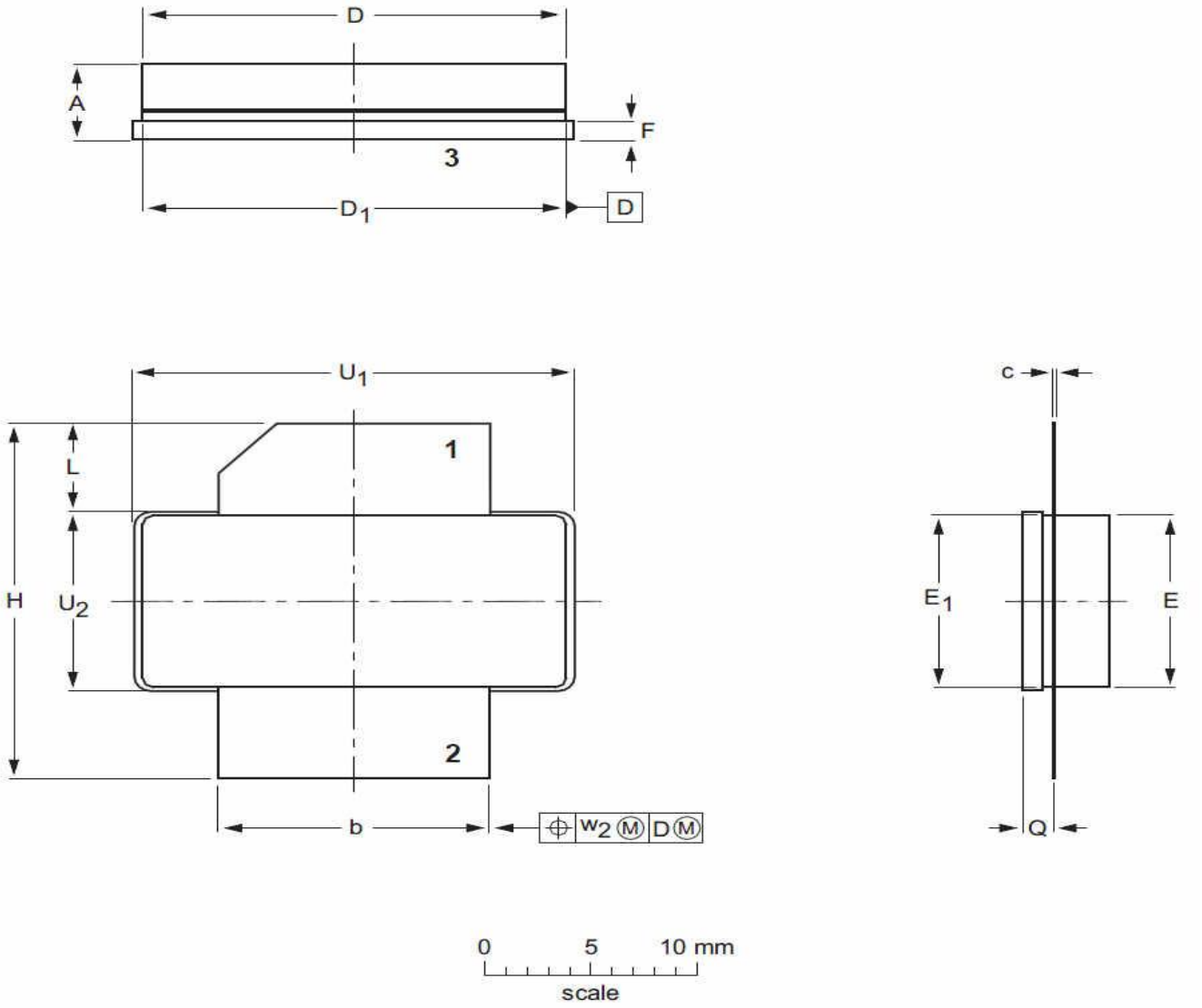


Figure 3. Power Gain，Efficiency as function of Pout



Earless flanged ceramic package; 2 leads（1—DRAIN、2—GATE、3—SOURCE）



UNIT	A	b	c	D	D_1	E	E_1	F	H	L	Q	U_1	U_2	W_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	1.70 1.45	20.70 20.45	9.91 9.65	0.25
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.067 0.057	0.815 0.805	0.390 0.380	0.010

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B2					03/12/2013

Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2026/3/3	**V1.0**	**Preliminary Datasheet**

Application data based on LSM-26-06

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