

STAH50095F4C GaN TRANSISTOR

Document Number:
STAH50095F4C
Preliminary Datasheet V1.0

Gallium Nitride 28V 95W, C band RF Power Transistor

Description

The STAH50095F4C is a 95W internally matched, GaN HEMT, designed from 4.4 to 5.0GHz, especially 5G NR or LTE application, as well as either Pulse or CW application. There is no guarantee of performance when this part is used in applications designed Outside of these frequencies.



- Typical **CW** performance (on 4.4-5GHz fixture with device soldered):

V_{ds}=28V, I_{bq}=100mA, CW

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff (%)	P1dB Gain (dB)	P3dB (dBm)	P3dB (W)	P3dB Eff (%)
4400	49.09	81.1	53.7	11.93	49.95	98.8	56.1
4500	49.16	82.4	53.9	12.72	50.07	101.7	56.2
4600	49.38	86.8	54.9	12.89	50.2	104.6	56.5
4700	49.36	86.2	55.4	13.06	50.19	104.5	57.0
4800	49.01	79.6	55.3	13.31	50	100.1	57.5
4900	48.8	75.8	54.7	12.96	49.82	95.9	56.8
5000	48.66	73.4	54.0	12.08	49.8	95.4	56.6

Applications and Features

- Suitable for wireless communication infrastructure, wideband amplifier, EMC testing, ISM etc.
- High Efficiency and Linear Gain Operations
- Thermally Enhanced Industry Standard Package
- High Reliability Metallization Process
- Excellent thermal Stability and Excellent Ruggedness
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

Turning the device ON

1. Set V_{GS} to the pinch-off (V_P) voltage, typically -5 V
2. Turn on V_{DS} to nominal supply voltage (28V)
3. Increase V_{GS} until I_{DS} current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce V_{GS} down to V_P, typically -5 V
3. Reduce V_{DS} down to 0 V
4. Turn off V_{GS}

Figure 1: Pin definitions (Top view)

Because of internal configuration, it must be used as single ended device.

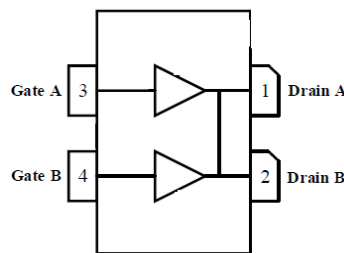


Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V _{DSS}	150	Vdc

STA50095F4C GaN TRANSISTOR

Document Number:
STA50095F4C
Preliminary Datasheet V1.0

Gate--Source Voltage	V_{GS}	-10,+2	Vdc
Operating Voltage	V_{DD}	36	Vdc
Maximum Forward Gate Current @ $T_c = 25^\circ\text{C}$	I_{gmax}	36	mA
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Case Operating Temperature	T_c	+150	$^\circ\text{C}$
Operating Junction Temperature(See note 1)	T_j	+225	$^\circ\text{C}$
Total Device Power Dissipation (Derated above 25°C , see note 2)	P_{diss}	150	W

Note: 1. Continuous operation at maximum junction temperature will affect MTTF
2. Bias Conditions should also satisfy the following expression: $P_{diss} < (T_j - T_c) / R_{JC}$ and $T_c = T_{case}$

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case $T_c = 85^\circ\text{C}$, $T_j = 200^\circ\text{C}$, RF CW operation	$R_{\theta JC}$	0.9	C/W

Table 3. Electrical Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise noted)

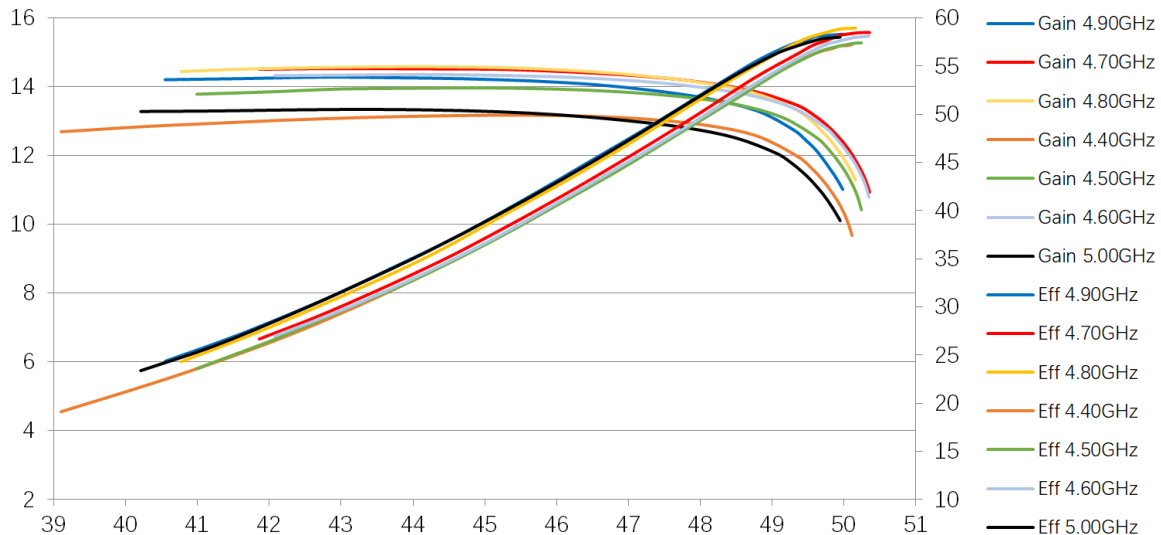
DC Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS} = -8\text{V}$; $I_{DS} = 25.2\text{mA}$	V_{DSS}	150			V
Gate Threshold Voltage	$V_{DS} = 28\text{V}$, $I_D = 25.2\text{mA}$	$V_{GS(th)}$	-4		-2	V
Gate Quiescent Voltage	$V_{DS} = 28\text{V}$, $I_{DS} = 200\text{mA}$, Measured in Functional Test	$V_{GS(Q)}$		-3.16		V

Typical performance

4.4-5GHz

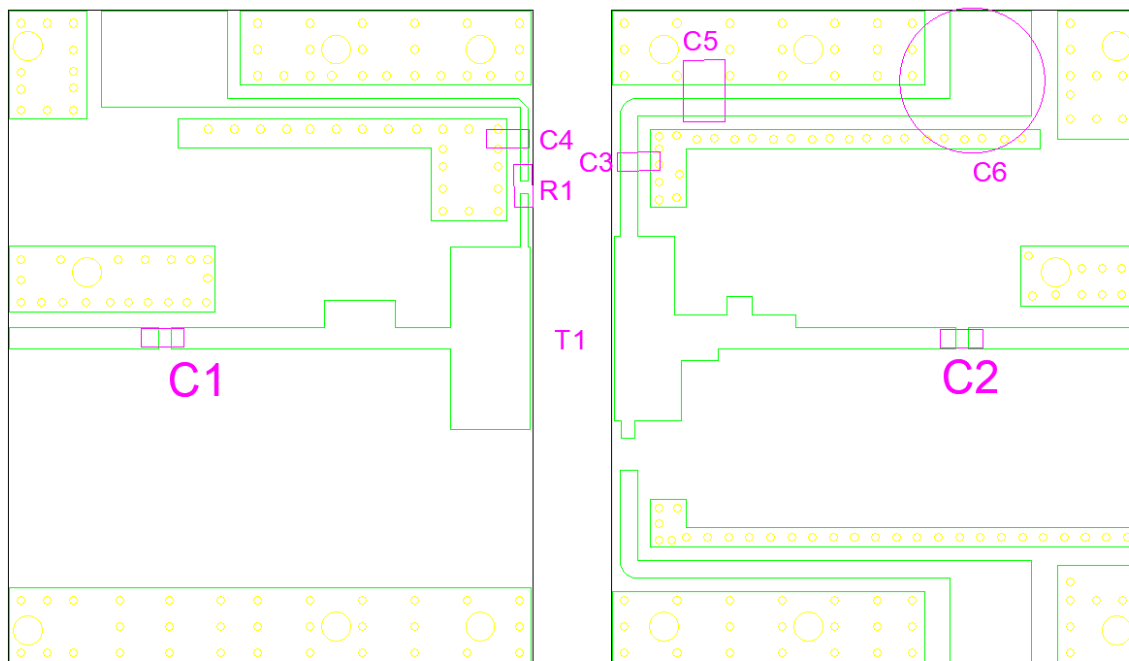
Figure 2: Power gain,efficiency as function of P_{out} , $V_{DS} = 28\text{V}$, $I_{DQ} = 100\text{mA}$ $V_{GS-main} = -3.13\text{V}$



STAH50095F4C GaN TRANSISTOR

Document Number:
STAH50095F4C
Preliminary Datasheet V1.0

Figure 3: Picture and Bill of materials of application circuit
(Layout Gerber file upon request)



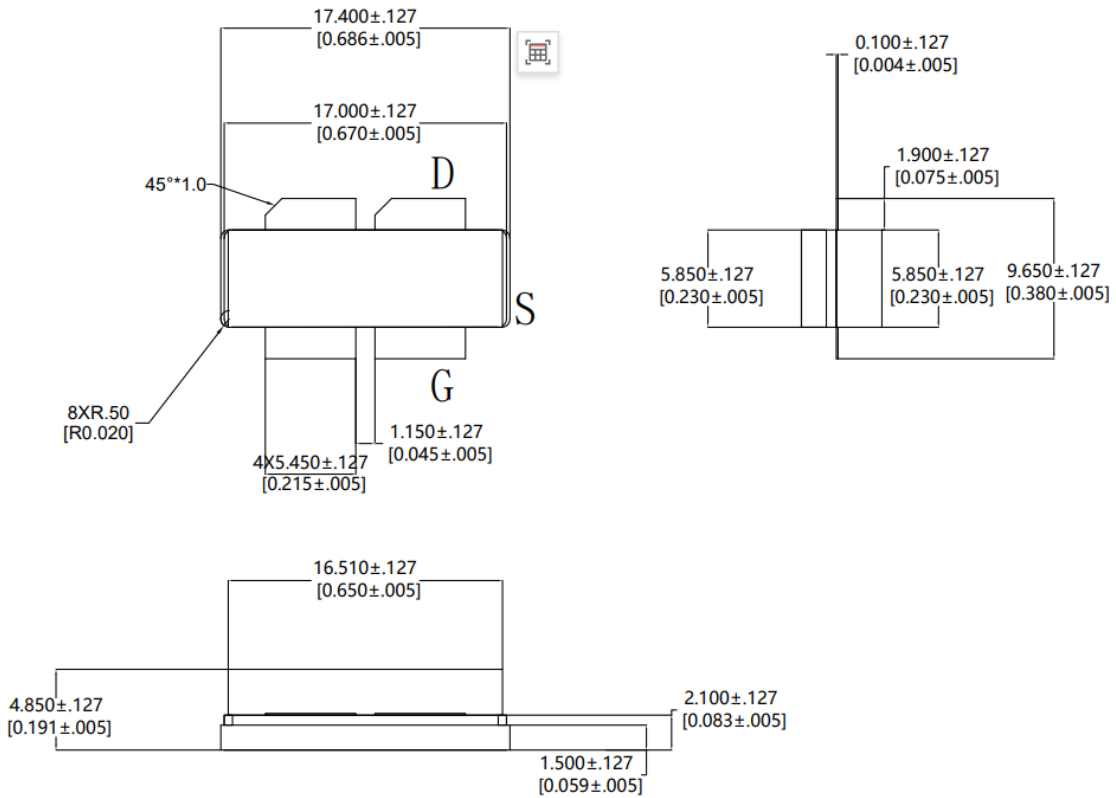
Part	Quantity	Description	Part Number	Manufacture
C1,C4	2	3.9pF High Q Capacitor	251SHS3R9BSE	TEMEX
C2,C3	2	8.2pF High Q Capacitor	251SHS8R2BSE	TEMEX
C5	1	10uF MLCC	GRM32EC72A106ME 05	Murata
C6	1	470UF		
R1	1	10 Ω Power Resistor	ESR03EZPF100	ROHM
T1	1	95W GaN Transistor	STAH50095F4C	Innogration

STA50095F4C GaN TRANSISTOR

Document Number:
STA50095F4C
Preliminary Datasheet V1.0

Package Outline

Flangeless ceramic package; 4 leads



OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-LBS					07/31/2023

Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2026/3/3	V1.0	Preliminary Datasheet Creation

Application data based on LWH-26-04