

MF012K6UPX LDMOS TRANSISTOR

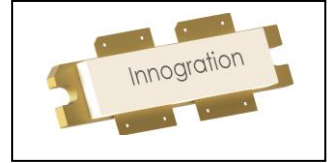
Document Number: MF012K6UPX
Preliminary Datasheet V1.0

2300W/2600W, 50V/60V High Power LDMOS FETs

MF012K6UPX

Description

The MF012K6UPX is a 50V/60V 2300W/2600W capable, high performance, unmatched LDMOS FET, designed for commercial and industrial applications with frequencies HF to 225MHz. It can be used for both CW and pulse application. It is featured for high power and high ruggedness, suitable for Industrial, Scientific and Medical application, as well as FM radio, HF communication, VHF TV and Aerospace applications.



Please notice that due to internal configuration of both input and output leads, dual path of this device must be configured as in-phase combination, NOT 180 degree Balun or 90 degree hybrid combination.

- Typical Performance (On Innogration in-phase combiner narrowband fixture with device soldered):

$V_{DD} = 50$ Volts, $I_{DQ} = 300$ mA, CW

Freq(MHz)	Pin(dBm)	Pout(W)	Gain(dB)	Eff(%)
13.56	42.5	2400	22	82

Load mismatch/Ruggedness test, result : **passed**

Freq(MHz)	Signal	VSWR	Pout (W)	Voltage(V)
13.56	CW	80:1 at all phase	2600	55

Features

- High Efficiency and Linear Gain Operations
- On chip RC network enable high stability and ruggedness
- Integrated ESD Protection
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Excellent thermal stability, low HCI drift
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	165	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+60	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_c	+150	°C
Operating Junction Temperature	T_j	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case ,Case Temperature 85°C, 2300W CW, 50 Vdc, $I_{DQ} = 70$ mA	$R_{\theta JC}$	0.10	°C/W
Transient thermal impedance from junction to case $T_j = 150^\circ$ C; $t_p = 100$ us; Duty cycle = 20 %	Z_{th}	0.015	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics ($T_A = 25^\circ$ °C unless otherwise noted)

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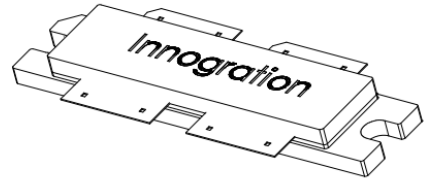
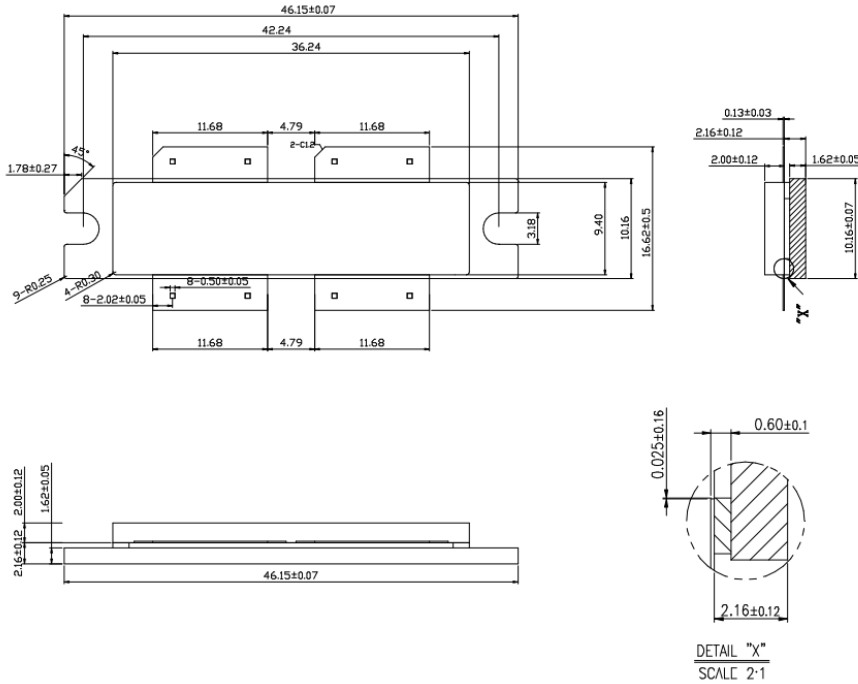
Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage $V_{GS}=0, I_{DS}=20.0\text{mA}$	$V_{(BR)DSS}$		165		V
Zero Gate Voltage Drain Leakage Current $(V_{DS} = 50\text{V}, V_{GS} = 0\text{V})$	I_{DSS}	—	—	1	μA
Gate—Source Leakage Current $(V_{GS} = 10\text{V}, V_{DS} = 0\text{V})$	I_{GSS}	—	—	1	μA
Gate Threshold Voltage $(V_{DS} = 50\text{V}, I_D = 600\ \mu\text{A})$	$V_{GS(th)}$	—	2.54	—	V
Gate Quiescent Voltage $(V_{DD} = 50\text{V}, I_D = 70\text{mA}, \text{Measured in Functional Test})$	$V_{GS(Q)}$	—	3	—	V

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Package Outline

Flanged ceramic package;



Unit:mm

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-O4E					5/6/2024

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Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2026/3/5	Rev 1.0	Preliminary Datasheet

Application data based on SYX-26-13

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