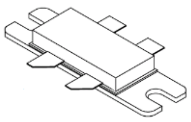
MK011K1VPX LDMOS TRANSISTOR

Document Number: MK011K1VPX
Preliminary Datasheet V1.0

1100W, 50V High Power RF LDMOS FETs

MK011K1VPX



Description

The MK011K1VPX is a 1100W capable, highly rugged, unmatched LDMOS FET, designed for commercial and industrial applications with frequencies HF to 200MHz

It is featured for industry leading high power and high ruggedness, suitable for Industrial, Scientific and Medical application, as well as HF communication, VHF TV and Aerospace applications.

- Application data at multiple frequencies

Freq(MHz)	Voltage(V)/Idq(mA)	Signal type	Pin(dBm)	Pout(W)	Power Gain(dB)	Eff(%)
108	50/200	CW	43	1100	17.5	80

Features

- High breakdown voltage enable possible class E operation at lower Vdd
- High Efficiency and Linear Gain Operations
- On chip RC network enable high stability and ruggedness
- Integrated ESD Protection
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Excellent thermal stability, low HCI drift
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain—Source Voltage	V_{DSS}	140	Vdc
Gate—Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case ,Case Temperature 85°C, 1100W CW, 50 Vdc, I_{DQ} = 240 mA	$R_{\theta JC}$	0.18	°C/W
Transient thermal impedance from junction to case Tj = 150° C; tp = 100 us; Duty cycle = 20 %	Zth	0.026	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22—A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage V_{GS}=0V, I_{DS}=1.0Ma	$V_{(BR)DSS}$		140		V
Zero Gate Voltage Drain Leakage Current	I_{DSS}	——	——	1	μA

(V_{DS} = 50V, V_{GS} = 0 V)					
Gate—Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600 μA)	$V_{GS(th)}$	——	2.54	——	V
Gate Quiescent Voltage (V_{DD} = 50 V, I_D = 180 Ma, Measured in Functional Test)	$V_{GS(Q)}$	——	3.1	——	V
Drain source on state resistance (V_{DS} = 0.1V, V_{GS} = 10 V) Each section side of device measured	Rds(on)		180		mΩ
Common Source Input Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz) Each section side of device measured	C_{ISS}		580		pF
Common Source Output Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz) Each section side of device measured	C_{OSS}		140		pF
Common Source Feedback Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz) Each section side of device measured	C_{RSS}		3.5		pF

TYPICAL CHARACTERISTICS (108MHz)

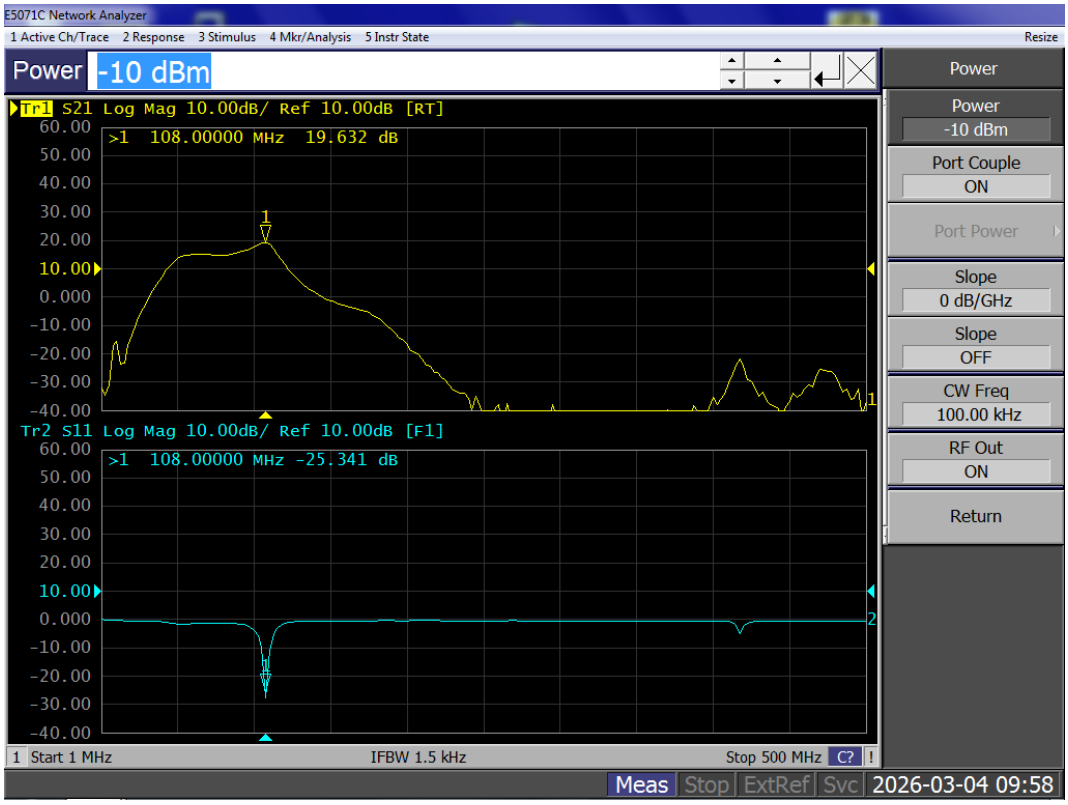


Figure 1: Network analyzer output S21/S11 (Vds=50V, Idq=1400mA)

Reference Circuit of Test Fixture (108MHz Power Amplifier)

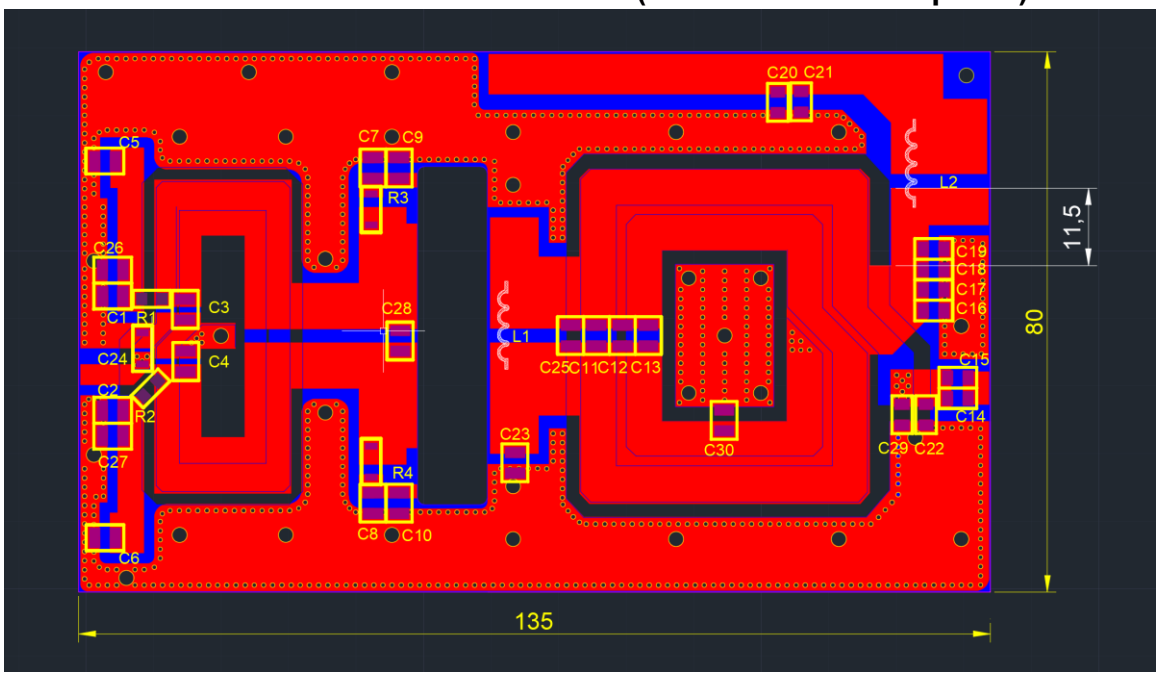
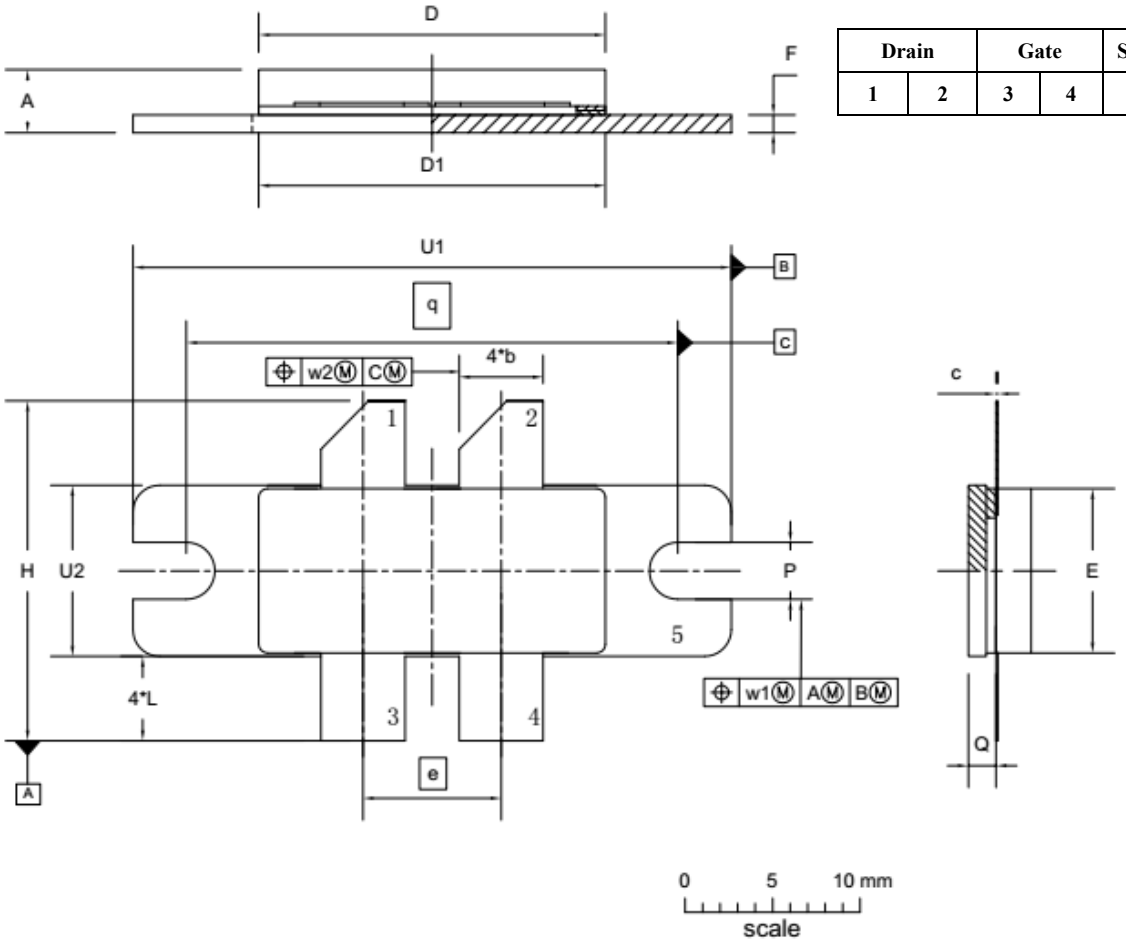


Table 5. Test Circuit Component Designations and Values

Component	Description	Suggested Manufacturer
C1~C4,C16~C19	560pF MQ301111	
C5,C6,C20,C21	10uF 1210	
C7,C8	910pF MQ301111	
C9,C10	470pF MQ301111	
C12,C11	15pF / 300V	
C13,C23,C30	18pF / 300V	
C25	9.1pF / 300V	
C24	82pF / MQ101111	
C22	4.7pF / MQ101111	
C28	270pF / MQ101111	
C29	0.8pF / MQ101111	
C26,C27	15pF / MQ101111	
C14,C15	680pF / MQ101111	
R1,R2	360Ω 1206	/
R3,R4	51Ω 2512	/
L1	2.5mm wire ， 8mm inner diameter, 3Turns	DIY
L2	2.5mm wire ， 8mm inner diameter, 4Turns	DIY

Package Outline

Eared Flanged Ceramic Package; 2 mounting holes; 4 leads



Drain		Gate		Source
1	2	3	4	5

UNIT	A	b	c	D	D_1	e	E	F	H	L	p	Q	q	U_1	U_2	W_1	W_2
mm	4.72 3.43	4.93 4.67	0.15 0.08	20.02 19.61	19.96 19.66	7.90	9.50 9.30	1.14 0.89	19.94 18.92	5.33 4.32	3.38 3.12	1.70 1.45	27.94	34.16 33.91	9.91 9.65	0.25	0.51
inches	0.186 0.135	0.194 0.184	0.006 0.003	0.788 0.772	0.786 0.774	0.311	0.374 0.366	0.045 0.035	0.785 0.745	0.210 0.170	0.133 0.123	0.067 0.057	1.100	1.345 1.335	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B4E					03/12/2013

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2026/3/5	Rev 1.0	Preliminary Datasheet

Application data based on SYX-26-12

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