



# GaN 50V, 400W, 2.4-2.5GHz RF Power Transistor

## Description

The STBV25402BY2 is a single ended 400watt capable, GaN HEMT, ideal for ISM applications within full band of 2.4-2.5GHz

There is no guarantee of performance when this part is used outside of stated frequencies.

- Typical CW performance at 2.4-2.5GHz applications

V<sub>DD</sub> = 50 Vdc, V<sub>GS</sub> = -5V, with device soldered, CW, P<sub>out</sub> defined with no I<sub>g</sub> leakage

Freq (MHz)	P <sub>out</sub> (dBm)	P <sub>out</sub> (W)	Gain-P <sub>out</sub> (dB)	I <sub>ds</sub> (A)	Eff (%)
2400	56.20	417	14.50	11.16	74.73
2450	56.25	422	14.65	11.29	74.75
2500	56.18	415	14.98	11.05	75.11

Recommended driver: STAV58016P2

## Applications

- 2.45GHz RF Energy
- S band power amplifier

### Important Note: Proper Biasing Sequence for GaN HEMT Transistors

#### Turning the device ON

1. Set V<sub>GS</sub> to the pinch-off (V<sub>P</sub>) voltage, typically -5 V
2. Turn on V<sub>DS</sub> to nominal supply voltage
3. Increase V<sub>GS</sub> until I<sub>DS</sub> current is attained
4. Apply RF input power to desired level

#### Turning the device OFF

1. Turn RF power off
2. Reduce V<sub>GS</sub> down to V<sub>P</sub>, typically -5 V
3. Reduce V<sub>DS</sub> down to 0 V
4. Turn off V<sub>GS</sub>

**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain--Source Voltage	V <sub>DSS</sub>	+200	Vdc
Gate--Source Voltage	V <sub>GS</sub>	-8 to +0.5	Vdc
Operating Voltage	V <sub>DD</sub>	55	Vdc
Maximum gate current	I <sub>gs</sub>	64.5	mA
Storage Temperature Range	T <sub>stg</sub>	-65 to +150	°C
Case Operating Temperature	T <sub>C</sub>	+150	°C
Operating Junction Temperature	T <sub>J</sub>	+225	°C

**Table 2. Thermal Characteristics**

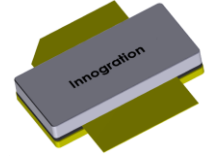
Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case by FEA T <sub>C</sub> = 25°C, at Pd = 140W	R <sub>θJC</sub>	0.6	°C /W

**Table 3. Electrical Characteristics (TA = 25°C unless otherwise noted)**

DC Characteristics (Each path, measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V <sub>GS</sub> = -8V; I <sub>DS</sub> = 64.5mA	V <sub>DSS</sub>		200		V
Gate Threshold Voltage	V <sub>DS</sub> = 10V, I <sub>D</sub> = 64.5mA	V <sub>GS(th)</sub>	-4	-	-2	V

**STBV25402BY2**





Gate Quiescent Voltage	VDS =50V, IDS=100mA, Measured in Functional Test	V <sub>GS(Q)</sub>		--3.2		V
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**Ruggedness Characteristics**

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Load mismatch capability	2.45GHz, Pout=400W pulse CW All phase, No device damages	VSWR		10:1		

**TYPICAL CHARACTERISTICS**

Figure 1: Efficiency and power gain as function of Pout

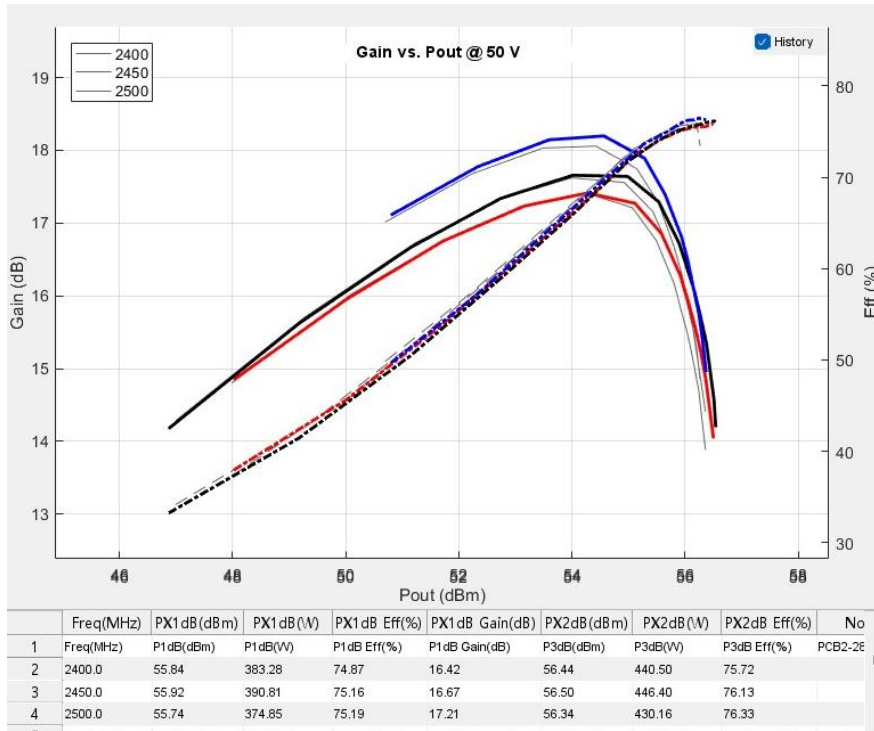
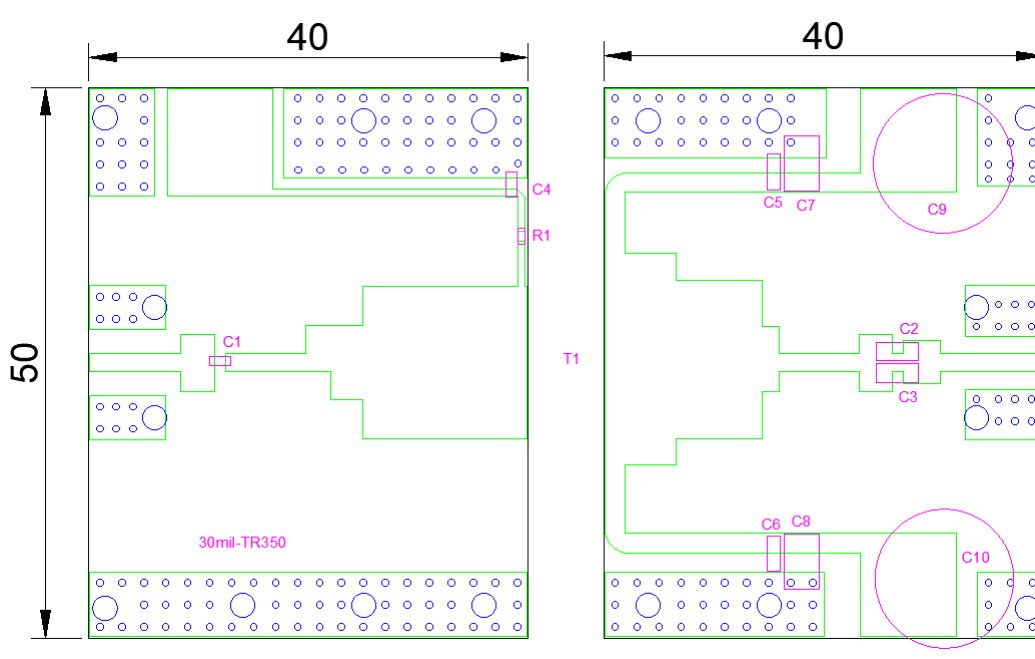


Figure 3: Reference design circuit (30mil TC350, PCB DWG file upon request,)



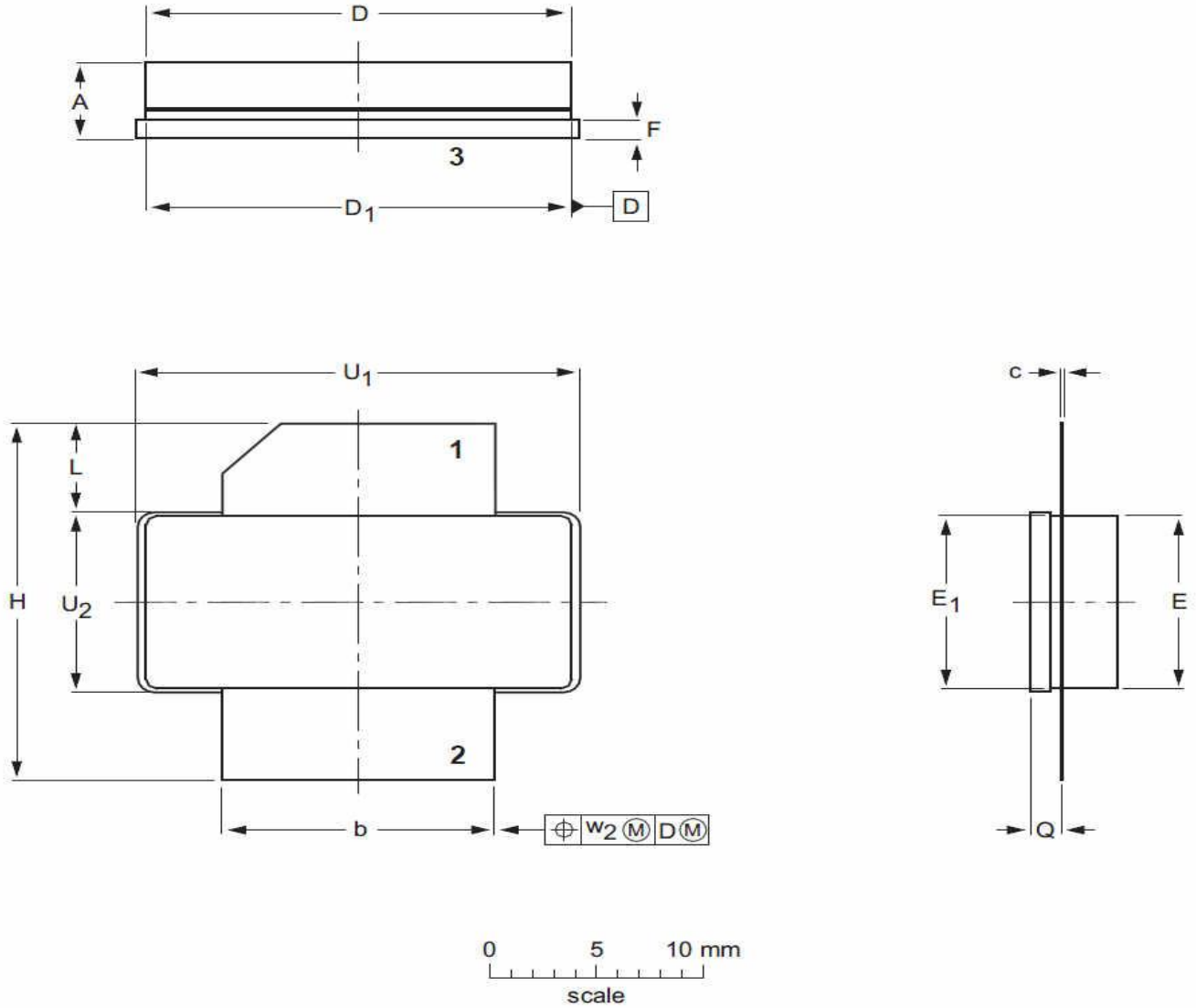


<b>Part</b>	<b>Quantity</b>	<b>Description</b>
C1, C4,C5,C6	4	12pF High Q Capacitor
C2,C3	2	6.8pF High Q Capacitor
C9,C10	2	1000uF/63V
C7,C8	2	10uF MLCC
R1	1	10 $\Omega$ Power Resistor



### Package Outline

Earless flanged ceramic package; 2 leads (1—DRAIN、2—GATE、3—SOURCE)



UNIT	A	b	c	D	D <sub>1</sub>	E	E <sub>1</sub>	F	H	L	Q	U <sub>1</sub>	U <sub>2</sub>	W <sub>2</sub>
mm	4.72	12.83	0.15	20.02	19.96	9.50	9.53	1.14	19.94	5.33	1.70	20.70	9.91	0.25
	3.43	12.57	0.08	19.61	19.66	9.30	9.25	0.89	18.92	4.32	1.45	20.45	9.65	
inches	0.186	0.505	0.006	0.788	0.786	0.374	0.375	0.045	0.785	0.210	0.067	0.815	0.390	0.010
	0.135	0.495	0.003	0.772	0.774	0.366	0.364	0.035	0.745	0.170	0.057	0.805	0.380	

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B2					03/12/2013



## Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2026/3/6	V1.0	Preliminary Datasheet Creation

Application data based on: LWH-26-05

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